TECHNICAL MANUAL

OPERATOR'S, ORGANIZATIONAL,

DIRECT SUPPORT, GENERAL SUPPORT, AND

DEPOT MAINTENANCE MANUAL

FOR

MONITOR AND TEST GROUP

COUNTERMEASURES RECEIVING SET

AN/FLR-9(V7)/(V8)

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TECHNICAL MANUAL

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OPERATOR'S, ORGANIZATIONAL, DIRECT SUPPORT, GENERAL SUPPORT, AND DEPOT MAINTENANCE MANUAL FOR

MONITOR AND TEST GROUP COUNTERMEASURES RECEIVING SET AN/FLR-9(V7)/(V8)

F & M SYSTEMS CO.

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SECTION I

DESCRIPTION

1-1. Scope.

This three volume manual describes the monitor and test group used in the Countermeasures Receiving Sets AN/FLR-9(V7)/(V8). Manual coverage consists of installation, operation, theory of operation, maintenance and repair, depot inspection standards, diagrams, parts list, and a from-to wire list. Coverage includes normal and emergency operation, replacement of parts, troubleshooting procedures; alignment procedures, and repair for all levels of maintenance. The operation/maintenance sections are contained in volume 1; the parts list is contain in volume 2, wire list in volume 3.

1-2. Purpose of Manual.

This manual is provided to instruct personnel in the operation and maintenance of equipment provided for the monitor and test group of the Countermeasures Receiving Sets AN/FLR-9(V7) and (V8).

1-3. Description and Purpose. (See figures 1-1 through 1-5.)

a. General Description. The monitor and test group (figure 1-1) is an integral part of the AN/FLR-9(V) system that is designed to check equipment performance during operation. The monitor and test group is composed of two subgroups; these are the on-line monitor and test (olm&t), and monitor (somc). The monitor and test subgroup (figures 1-2 through 1-4) performs voltage, phase, and frequency measurement functions. The monitor subgroup (figure 1-5) provides equipment malfunction alarms, status indications, and control of olm&t tests. Testing is performed under the system control group computer control. Results are provided in the form of teletypewriter (tty) machine printouts. The printouts identify the test and give results, fault locations, date, and time information. The test routine selects the rf path to be tested by switching the beamformer element test matrix (see figure 7-5). Next, a predetermined test signal frequency is selected by the oscillator select matrix. This test signal is then injected into the selected rf path by directional couplers. After the signal has traveled through the selected path, the test signal is coupled to the beamformer test output matrix and then to the measuring equipment. The measuring equipment provides for measuring output amplitude, output phase, and output frequency. Monitoring and testing is performed while the FLR-9 System is in operation without affecting the FLR-9 operations. Operations at a position can only be affected if the frequency being monitored is very close to the test oscillator frequency. Should the frequency being monitor be at the frequency of the test oscillator, the short duration of the test signal (approximately 80 milliseconds) would not be discernible. Six frequencies are provided in each band to provide test flexibility. The Console, Operation and Maintenance OJ-263/FLR-9(V) (somc) operator can select the frequency to be used in each band.

b. Olm&t Tests. There are four groups of olm&t tests. These are the antenna elements verification, the beamformer amplitude and delay verification, the switch matrix crosspoint verification, and the oscillator frequency test. Each is a separate and complete routine which can be initiated by the somc operator.

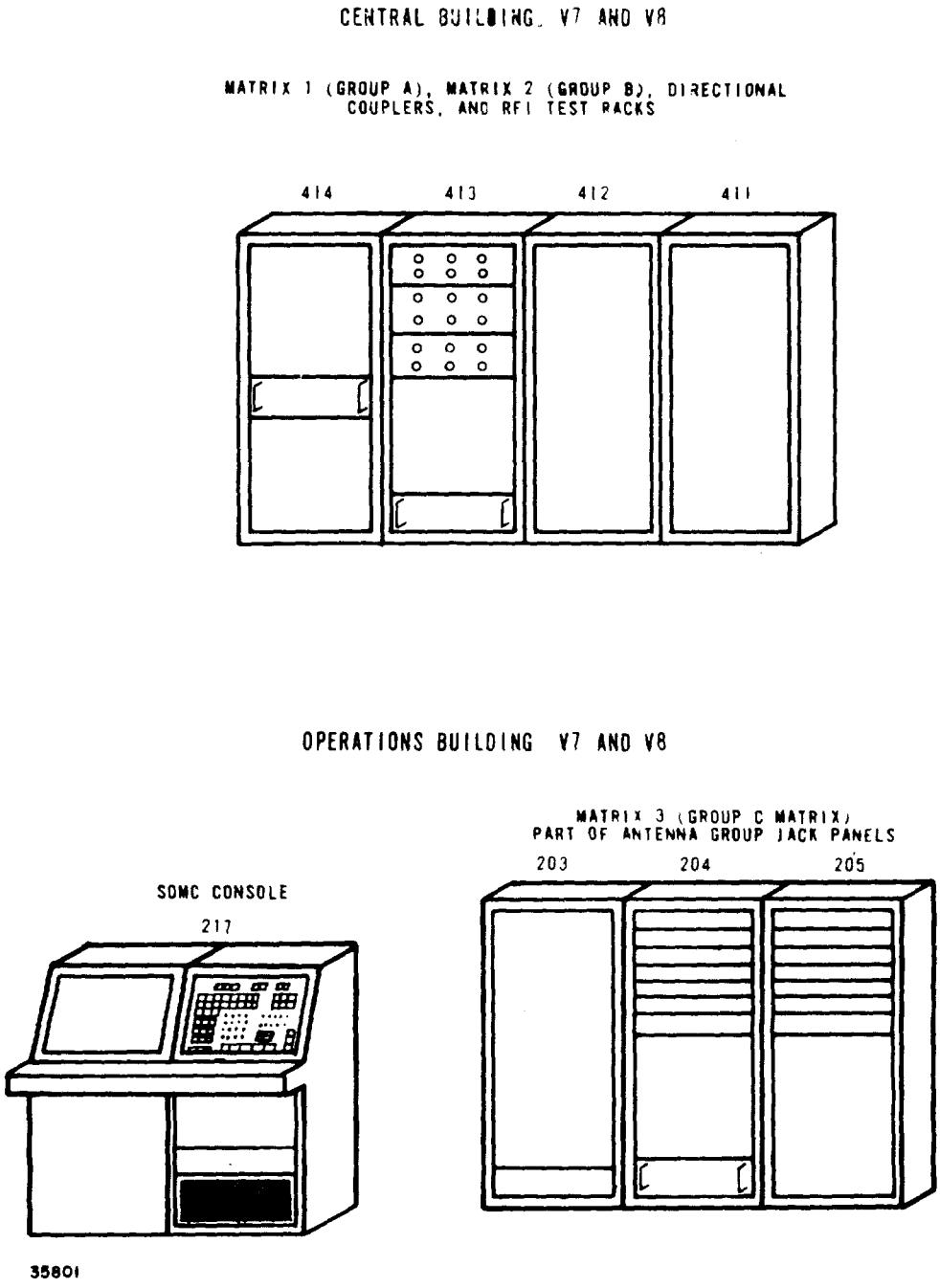

Figure 1-1. Monitor and Test Group, V7 and V8

Table 1-1. Leading Particulars (Continued)

Qty Site	Item	Primary Power Requirements	Dimensions*			Weight
			Height	Width	Depth	
1	Power divider panel 3300-44096.	None.	7.0 Inches	19.0 inches	2.0 inches	5 pounds
2	Analog-to-digital converters, 52100 and 52100-1.	Requires 105 through 132 volts ac at 48-Hz through 63-Hz input voltage. Input current is 1.0 ampere.	5-1/4 inches	19.0 inches	16.0 inches	40 pounds
1	Frequency counter H33-5245M.	Requires 115 volts or 203 volts ±10 percent at 50-Hz to 60-Hz input voltage. Input current is 1.0 ampere.	5-1/4 inches	19.0 inches	16.0 inches	32 pounds
3	Bandpass filter assembly panels, 3300-44093.	None.	8-3/4 inches	19.0 inches	2.0 inches	7 pounds
2	Line filter LMF-1283.	Incoming power is 105 through 132 volts ac.	22-1/2 inches	4-1/2 inches	4-1/2 inches	21 pounds
1	Group B matrix (4 each assemblies), 503855.	None.	12-1/4 inches	19.0 inches	8.0 inches	80 pounds
3	Reference oscillator assemblies, 3300-44038.	Requires input power of 105 through 132 volts ac at 48 through 63 Hz. Input current 1.0 ampere.	8-3/4 inches	19.0 inches	17.0 inches	40 pounds
1	Group A matrix (5 each assemblies), 503854.	None.	12-1/4 inches	19.0 inches	8.0 inches	100 pounds
1	Alarm junction box.	None	3-1/2 inches	19.0 inches	6.0 inches	5 pounds

*Each assembly

Table 1-1. Leading Particulars (Continued)

Qty Site	Item	Primary Power Requirements	Dimensions*			Weight
			Height	Width	Depth	
1	Power supply number i, 3300-44100.	105 through 132 volts ac at 1.1 amperes, 48 through 63 Hz.	7.0 inches	19.0 inches	23.0 inches	40 pounds
1	Group C matrix (6 each assemblies), Site V8, 503856.	None.	12-1/4 inches	19.0 inches	10.0 inches	120 pounds
1	Group C matrix (4 each assemblies), Site V7, 503873.	None.	12-1/4 inches	19.0 inches	10.0 inches	80 pounds
1	Power supply number 2 (V7), 3300-44101.	105 through 132 volts ac at 48 through 63 Hz. Input current is 1.6 amperes.	7.0 inches	19.0 inches	23.0 inches	23 pounds
1	Power supply number 3 (V8), 3300-44102.	105 through 132 volts ac at 48 through 63 Hz. Input current is 2.5 amperes.	7.0 inches	19.0 inches	23.0 inches	51 pounds
1	Somc, 3300-46170 (V8), 3300-46112(V7).	None	19-1/4 inches	19.0 inches	3.0 inches	10 pounds
1	Blower unit, cabinet cooling, R2EB412A37.	108 through 132 volts ac at 48 through 63 Hz, 2.5 amperes.	7.0 inches	19.0 inches	10-1/2 inches	15 pounds
1	Controller, somc 3300-46050.	None.	12.0 inches	19.0 inches	6.0 inches	12 pounds
1	Power supply assembly, -6 volts, somc 3300-46071.	108 through 132 volts ac at 48 through 63 Hz, 0.5 ampere.	4.0 inches	19.0 inches	6.0 inches	6 pounds
1	Power supply assembly, dual, somc 3300-46119.	108 through 132 volts ac at 48 through 63 Hz, 6.0	8.0 inches	19.0 inches	23.0 inches	80 pounds

Table 1-1. Leading Particulars (Continued)

Qty Site	Item	Primary Power Requirements	Dimensions			Weight
			Height	Width	Depth	
1	Fuse panel, 3300-46163.	None.	3.0 inches	19.0 inches	3.0 inches	2 pounds
1	Panel, shield return, 3300-46120.	None.	3.0 inches	19.0 inches	1.0 inches	1 pound
1	Panel, power distri-bution, somc, 3300-46130.	None.	3.0 inches	19.0 inches	1.0 inches	1 pound

Table 1-2. Capabilities and Limitations

Item	Parameter	Description
Monitor and test group	Tests performed	Four olm&t system reports initiated from the somc control panel Path verification, automatic; initiated by a beam request. Individual tests as desired are initiated at the tty terminals.
	Readout of test results	Test results, alarms, and malfunction information are output on the tty terminal. Olm&t system reports can also be recorded on magnetic tape.
	System parameters tested	Voltage, phase, frequency
	System controls	CPU PRIMARY SELECT CPU OFF-LINE I/0 BUS SWITCH MANUAL OVERRIDE CPU CHANGEOVER INHIBIT
	Monitor indicators	
	Airflow alarms	16 for site V7, 16 for site V8
	Temperature alarms	21 for site V7, 39 for site V8
	Equipment failure alarms	23 for site V7, 25 for site V8
	Status indicators	Two each for magnetic tape handlers, two each for tty units, 12 each for cpu status
	Test frequencies	Provides six test oscillator frequencies per band for each of three bands. Band A uses frequencies 1.5, 2.0, 3.0, 3.5, 4.5, and 6.0 MHz. Band B uses frequencies 6.0, 7.5, 9.0, 12.0, 14.0, and 18.0 MHz. Band C uses frequencies 18.0, 19.0, 22.0, 24.0, 27.0, and 30.0 MHz.

Table 1-2. Capabilities and Limitations (Continued)

Item	Parameter	Description
Test oscillators CO-211LD	Type	Crystal controlled, sealed unit
	Stability	1 part in 10^8 per day ±2 parts in 10^9 for ±5-percent supply variation ±1 part in 10^9 for 10-percent load variation ±1 part in 10^8 over -20°C to +71°C temperature range
Oscillator power supply LM-CC-24	Output voltage	24 volts dc
	Input voltage	120 volts ac ±10 percent, 48 through 63 Hz
	Input current	Approximately 1 ampere
	Operating temperature	0°C to 55°C
Bandpass filter, 285B1 through 285B16	Impedance	75 ohms ±20 ohms
	Input signal level, normal	+4 dBm at 75 ohms
	Bandwidth	At 3-dB level, 0.025 percent of center frequency
	Insertion loss	Less than 4 dB at center frequency
	Phase shift	±360 degrees at center frequency
	Operating temperature	+15.60°C to +26.7°C
	Non-operating temperature	-54°C to +71.1° C
Rf attenuators 44063	Range	0 through 10 dB variable
	Impedance	75 ohms ±5 ohms
	Readout accuracy	±0.5 dB
	Average power input	2 watts
	Operating temperature	±15.6°C to +26.7°C
	Non-operating temperature	-54°C to +71.1°C
Rf power dividers and combiners 44873 and 44874	Input power level	+20 dBm or less
	Impedance	75 ohms unbalanced
	Frequency range	1.5 MHz to 30 MHz

Table 1-2. Capabilities and Limitations (Continued)

Item	Parameter	Description
	Operating temperature Non-operating temperature	+15.6°C to +26.7°C -54° C to +71.1° C
Analog-to digital con-verters 52100 T and 52100 T-1	Quantity used	Two each
	Ranges	One each converter at 0.0-volt dc to 1-volt dc full-scale conversion and one each at -0.5-volt dc to +0.5-volt dc full-scale conversion
	Input impedance	Greater than 10,000 ohms
	Output	Binary number, 12 bits wide at TTL logic levels
	Input power	48 to 62 Hz, 105-130 volt ac, 1 ampere
	Conversion rate	Not less than 10,000 per second
	Overall accuracy	0.025 percent ±1/2 LSB
	Line regulation accuracy	0.005 percent per 1-percent variation of primary power
	Operating temperature	+15°C to +26.7°C
	Non-operating temperature	-54°C to +71° C
Switching matrices groups A, B, and C	Input impedance	75 ohms
	Output impedance	75 ohms
	Path attenuation	Not greater than -1 dB ±0.5 dB
	Attenuation reference outputs	-10 dB
	Amplitude difference path-to-path	(Groups A and B) less than 0.25 dB
	Operating temperature	+15°C to +26.7°C
	Non-operating temperature	-54° C to +71° C
Vector voltmeter H16-8405A	Frequency range tuning	1 MHz to 1 GHz; automatic with 20-millisecond search and lock time
	Voltage range Channel A	1 to 10 MHz is 1.5 millivolts to 1 volt rms 10 to 500 MHz is 300 microvolts to 1 volt rms

Table 1-2. Capabilities and Limitations (Continued)

Item	Parameter	Description
	Channel B	100 microvolts to 1 volt rms 0.1 megohm shunted by 2 pf
	Voltage accuracy	2 percent of full scale
	Phase accuracy	±0.1-degree resolution, ±1.5-degree accuracy
	Phase range	-180 to +180 degrees
	Input power	115 or 230 volts ac ±10 percent, 50 to 400 Hz, 35 watts
	Operating temperature	+15°C to 55°C
Frequency counter H33-5245M	Frequency range	0 to 50 MHz
	Output	Eight digits of four-line bcd
	Input impedance	1 megohm shunted with 25 pf
	Accuracy	±1 count ± time base accuracy
	Time base	5 MHz
	Signal input	Minimum 100 millivolts rms to 10 volts rms
	Input power	115 or 230 volts ±10 percent, 50 to 60 Hz, 95 watts (150 watts maximum startup power)
	Operating temperature	-20°C to +65°C
Overvoltage protector LM-0V-1	Protection point	Adjusted to 155 percent of power supply voltage
	Adjustment range	3 to 8 volts dc
	Used on	Monitor and test group power supplies output 5 volts or 6 volts (not LM-EE)
Overvoltage protector LM-0V-2	Protection point	Adjusted to 115 percent of power supply voltage
	Adjustment range	6 to 20 volts dc
	Used on	Monitor and test group power supplies output 8 volts or 12 volts (not LM-EE)
Overvoltage protector LM-0V-3	Protection point	Adjusted to 115 percent of supply voltage
	Adjustment range	18 to 70 volts dc
	Used on	Monitor and test group power supplies output 24 volts or 28 volts (not LM-EE)

Table 1-2. Capabilities and Limitations (Continued)

Item	Parameter	Description
Overvoltage protector LM-OV-8	Protection point	Adjusted to 115 percent of supply voltage
	Adjustment range	6 to 20 volts dc
	Used on	Monitor and test group power supplies output 8 volts or 12 volts Used on the LM-EE package only
Overvoltage protector LM-OV-9	Protection point	Adjusted to 115 percent of supply voltage
	Adjustment range	18 to 70 volts dc
	Used on	Monitor and test group power supplies output 28 volts Used on the LM-EE package only
Power supply LM-B-5	Input power	105 to 132 volts ac at approximately 0.2 ampere
	Output voltage	5 volts dc
	Operating temperature	-20°C to 71°C
	Line regulation	Less than 0.05 percent plus 4.0 millivolts from 105 to 132 volts ac
	Load regulation	Less than 0.03 percent plus 3.0 millivolts from zero to full load
	Temperature regulation	0.03 percent per degree centigrade
	Ripple	1 millivolt rms
Power supply LM-CC-5	Input power	105 to 132 volts ac at approximately 0.5 ampere
	Output voltage	5 volts dc
	Operating temperature	-20°C to 71°C
	Line regulation	Less than 0.05 percent plus 4.0 millivolts from 105 to 132 volts ac
	Load regulation	Less than 0.03 percent plus 3.0 millivolts from zero to full load
	Temperature regulation	0.03 percent per degree centigrade
	Ripple	1 millivolt rms
Power supply LM-CC-8	Input power	105 through 132 volts ac at approximately 0.6 ampere
	Output voltage	8 volts dc
	Operating temperature	-20°C to 71° C

Table 1-2. Capabilities and Limitations (Continued)

Item	Parameter	Description
	Line regulation	Less than 0.05 percent plus 4.0 millivolts from 105 to 132 volts ac.
	Load regulation	Less than 0.03 percent plus 3.0 millivolts from zero to full load
	Temperature	0.03 percent per degree centigrade
	Ripple	1 millivolt ampere
Power supply LM-CC-24	Input power	105 to 132 volts ac at approximately 1.0 ampere
	Output voltage	24 volts dc
	Operating temperature	-20°C to 71°C
	Line regulation	Less than 0.05 percent plus 4.0 millivolts from 105 to 132 volts ac
	Load regulation	Less than 0.03 percent plus 3.0 millivolts from zero to full load
	Temperature regulation	0.03 percent per degree centigrade
	Ripple	1 millivolt rms
Power supply LM-EE-28	Input power	105 to 132 volts ac at approximately 4 amperes
	Output voltage	28 volts dc
	Operating temperature	-20°C to 71°C
	Line regulation	Less than 0.05 percent plus 4.0 millivolts from 105 to 132 volts ac
	Load regulation	Less than 0.03 percent plus 3.0 millivolts from zero to full load
	Temperature regulation	0.03 percent per degree centigrade
	Ripple	1 millivolt rms
Power supply LM-D-8	Input power	105 to 132 volts ac at approximately 1 ampere
	Output voltage	8 volts dc
	Operating temperature	-20°C to 71°C
	Line regulation	Less than 0.05 percent plus 4.0 millivolts from 105 to 132 volts ac
	Load regulation	Less than 0.03 percent plus 3.0 millivolts from zero to full load
	Temperature regulation	0.03 percent per degree centigrade
	Ripple	1 millivolt rms

Table 1-2. Capabilities and Limitations (Continued)

Item	Parameter	Description
Power supply LM-B-24	Input power	105 to 132 volts ac at approximately 0.4 ampere
	Output voltage	24 volts dc
	Operating temperature	-20°C to 71°C
	Line regulation	Less than 0.05 percent plus 4.0 millivolts from 102 to 132 volts ac
	Temperature regulation	0.03 percent per degree centigrade
	Ripple	1 millivolt rms
Power supply LM-EE-8	Input power	105 to 132 volts ac, 48 through 62 Hz at approximately 2.5 amperes
	Output voltage	8 volts dc
	Operating temperature	-20°C to 71°C
	Line regulation	Less than 0.05 percent plus 4.0 millivolts from 105 to 132 volts ac
	Load regulation	Less than 0.03 percent plus 3.0 millivolts from zero to full load
	Temperature regulation	0.03 percent per degree centigrade
	Ripple	1 millivolt rms
Power supply LM-258	Input power	105 to 132 volts ac, 48 to 62 Hz at approximately 0.5 ampere
	Output voltage	-7 volts dc at 1.2 amperes
	Operating temperature	-20°C to 71°C
	Line regulation	Less than 0.05 percent plus 4.0 millivolts from 105 to 132 volts ac
	Load regulation	Less than 0.03 percent plus 3.0 millivolts from zero to full load
	Temperature regulation	0.03 percent per degree centigrade
	Ripple	1 millivolt rms
	Adjustment range	0 to 15 volts dc
Power supply LM-E-5	Input power	105 to 132 volts ac, 45 to 440 Hz
	Output voltage	5 volts at 20 ampere maximum
	Operating temperature	-20°C to 710°C
	Line regulation	Less than 0.05 percent plus 4.0 millivolts from 105 to 132 volts ac

Table 1-2. Capabilities and Limitations (Continued)

Item	Parameter	Description
	Load regulation	Less than 0.03 percent plus 3.0 millivolts from zero to full load
	Temperature regulation	0.03 percent per degree centigrade
	Ripple	1 millivolt rms
	Voltage range	5 volts dc ±5 percent
Signal data converter	Signal inputs	
	Vvm control group	Four lines decoding to nine control signals
	Vvm unlock input	One input and one output
	Frequency meter data inputs	Thirty-two signal inputs of binary coded decimal, requesting eight digits of readout
	Signal outputs	
	Vvm control group	Nine control signals accomplished by grounding each control wire as selected
	Vvm unlock output	One line driver output to computer
	Frequency meter data	Thirty-two line driver outputs to the cable scan multiplexer
Power supply 3300-44037*	Input voltage	120 ±12 volts ac, 48 to 62 Hz, single phase
	Output voltage	5 volts dc ±0.5 volt dc
	Output current	4 amperes at 26.7°C derated to 3.2 amperes at 51.7° C
	Regulation	Combined line and load, 0.5 percent maximum
	Ripple and noise	50 millivolts rms maximum
	Ambient temperature	
	Operating	0°C to 26.7°C and 0°C to 51.7°C derated
	Non-operating	-54°C to 71°C
	Overvoltage protection	Set at 6 volts dc ±0.1 volt dc
	Stability	±20 millivolts/8 hours at constant line, load, and temperature
	Temperature Coefficient operating temperature range	0.03 percent per degree centigrade over

* Part of signal data converter

Table 1-3. Equipment Supplied

Nomenclature	Name	Function
3300-34002-1	Rfi test rack olm&t	Used to measure voltage, frequency and phase relationships of test signals supplied to it from the olm&t matrix 2 rack.
52100-1	Analog-to-digital converter	Converts the analog output of the vvm to a binary digit output; outputs to the cable scan multiplexer in the system control group; externally controlled by the matrix multiplexer in the system control group.
Converter, Signal Data CV-2977/FLR-9(v) (3300-44051-1)	Signal data converter	Provides line receivers and decoding for vvm control; provides line drivers for frequency counter output.
Power Supply PP-6813/FLR-9(V) (3300-44037-1)	Power supply	Provides +5-volt dc power for the signal data converter.
Divider Assembly, Power Rf CV-2048/FLR-9(V) (3300-44096-1)	Power divider assembly	Provides mounting surface for the power combiners (44874) and the power splitters (44873) that are part of the input circuitry to the vvm and the frequency counter.
	NOTE **See paragraph 1-9 for equipment location.**	
3300-44874-1	Power combiner	Makes one of three inputs into one output; first element of the input test circuit.
3300-44873-1	Power splitter	Makes one input into two outputs; divides each of the two input signals so that they may be measured on both test instruments.
LMF-1283	Line filter	Filters incoming power line; provides interference isolation.

Table 1-3. Equipment Supplied (Continued)

Nomenclature	Name	Function
3300-34003-1 coupler rack	Directional	Provides housing and mounting for the olm&t bandpass filters and output directional couplers.
Filter Assembly, Bandpass F-1337/FLR-9(V) (3300-44093-1 ,-2,-3)1	Bandpass filter assembly bands A, B, and C	Provides mounting for the olm&t bandpass filters; one assembly is provided for each of the three bands.
285B1 through B16	Bandpass filters	Narrow bandpass rf filters; one filter is provided for each of the 18 olm&t test oscillators.
3300-34001-1	Matrix 2 rack	Houses the group B matrices and olm&t test oscillators for bands A, B, and C.
3300-44177-1	Group B matrices, olm&t	Provides group B matrix signal path switching in the olm&t test circuits for bands A, B, and C.
Interface Unit Digital MX-9250/FLR-9(V) (3300-44175-2)	Digital interface unit, group B matrices	Provides switching signals for the band A, B, and C matrix assemblies.
3300-44168-1	Band A matrix, group B matrices	Provides band A matrix switching for group B functions.
3300-44167-1	Band B matrix, group B matrices	Provides band B matrix switching for group B functions.
3300-44166-1	Band C matrix, group B matrices	Provides band C matrix switching for group B functions.
Generator, Signal SG-lO01/FLR-9(V) (3300-44038-3) SG-1002/FLR-9(V) (3300-44038-2) SG-1 003/FLR-9(V) (3300-44038-)	Signal source generator assembly	One assembly is provided for each of the three bands; mounts six oscillators, six attenuators, and one power supply; provides oscillator signals for olm&t testing.
C0-211LD	Oscillator	Provides test signal at closely controlled frequency for olm&t testing.
3300-44063-1	Attenuator	Provides output amplitude control for olm&t test oscillators.

Table 1-3. Equipment Supplied (Continued)

Nomenclature	Name	Function
LM-CC-24	Power supply	Provides 24-volt dc supply voltage for olm&t test oscillators.
LM-OV-3	Overvoltage protector	Provides overvoltage protection for the oscillator circuits
3300-34004-1	Matrix 1 rack	Houses the group A matrices for bands A, B, and C; houses the alarm junction box and the power supply.
3300-44176-1	Group A matrices, olm&t	Provides group A matrix signal path switching in the olm&t test circuits for bands A, B, and C.
Interface Unit, Digital MX-9251/FLR-9(V) (3300-44175-1)	Digital interface unit, group A matrices	Provides switching signals for the band A, B, and C matrix assemblies.
3300-44170-1	Band A or C matrix, group A matrices	Provides band A or band C switching for group A functions.
3300-44171-1	Band B matrix, group A matrices	Provides half of the band B switching for group A functions; works with 3300-44169-1.
3300-44169-1	Band B matrix, group A matrices	Provides half of the band B switching for group A functions; works with 3300-44171-1.
3300-44111-1	Alarm junction box	Provides collection point for alarm circuits from equipment in the central building and to the somc in the operations building.
Power Supply PP-6811/FLR-9(V) (3300-44100-1)	Power supply number 1 assembly	Supplies power to the group A and B matrices and to the signal data converter in the olm&t equipment cabinets 411 through 414 in the central building.
LM-D-8	Power supply equipment.	Provides 8-volt dc supply to olm&t Part of 44100.
LM-CC-5	Power supply equipment.	Provides 5-volt dc supply to olm&t Part of 44100.
LM-OV-1,2, 8 and 9	Overvoltage protectors	Provides overvoltage protection for power supply circuits.

Table 1-3. Equipment Supplied (Continued)

Nomenclature	Name	Function
Site V7 3300-44179-1	Group C matrices olm&t	Provides group C matrix signal path switching in the olm&t test circuits; samples 400 inputs from the switching matrix and provides one output to the olm&t test circuitry in the central building.
Interface Unit, Digital MX-9248/FLR 9(V) (3300-44175-4)	Digital interface unit, group C matrices (V7)	Provides switching signals for the band A, B, and C matrices.
3300-44174-1	Sampling matrix, group C matrices (V7)	Provides part of the group C matrix switching; used with 3300-44173-1 matrix.
3300-44173-1	Sampling matrix, group C matrices	Provides part of the group C matrix switching; used with 3300-44174-1 matrices,
Site V8 3300-44178-1	Group C matrices, olm&t	Provides group C matrix signal path switching in the olm&t test circuits; samples 805 inputs from the switching matrix and provides one output to the olm&t test circuitry in the central building.
Interface Unit, Digital MX-9247/FL R-9(V) (3300-44175-3)	Digital interface unit, group C matrices (V8)	Provides switching signals for the band B, and C matrices.
3300-44174-1	Sampling matrix, group C matrices (V8)	Provides part of the group C matrix switching; used with 3300-44172-1 matrix.
3300-44172-1	Sampling matrix, group C matrices (V) 8	Provides part of the group C matrix switching; used with 3300-44174-1
Power Supply 00-6814/FLR-9(V) (3300-44102-1)	Power supply number 3 assembly, group C matrices (8)	Provides power for the operation of the the group C matrices at site V8.
LM-B-24	Power supply, 24-volt	Supplies 24 volts dc part of 44102.
LM-EE-8	Power supply, 8-volt	Supplies 8 volts dc part of 44102.

Table 1-3. Equipment Supplied (Continued)

Nomenclature	Name	Function
LM-B-5	Power Supply 5-volt	Supplies 5 volts dc part of 44102.
Power Supply PP-6810/FLR-9(V) (3300-44101-1)	Power supply number 2 assembly, group C matrices (V7)	Provides power for the operation of the group C matrices at site V7.
LM-B-24	Power supply, 24-volt	Supply 24 volts dc part of 44101.
LM-CC-8	Power supply, 8-volt	Supplies 8 volts dc part of 44101.
LM-B-5	Power supply, 5-velt	Supplies 5 volts dc part of 44101.
Console, Operation and Maintenance OJ-263/FLR-9(V) f3300-36005-1 (V7) 3300-36005-2 (V8)1	Somc	Provides hardware monitoring indicators for abnormal temperatures, cabinet air-flow or equipment failure; provides in-dicators and controls for computer functions.
Panel, Switching SA-1873/FLR-9(V) (3300-46170-1 and SA-1872/FLR-9(V) (3300-46112-1)	Control panel, somc (V8); Control panel, somc (V7)	Provides controls and indicators for operator use; indicators signal aud-ible and visual alarms and status; controls manipulate computer status and request olm&t test.
3300-46050-1	Controller, somc	Provides line drivers, receivers, and signal conditioning for the operation of the controls and indicators on the control panel.
Power Supply PP-6809/FLR-9(V) (3300-46071-1)	Power supply assembly, -7 volts somc	Supplies -7 volts to the somc control panel clock input.
LM258	Power supply, -7 volts	Supplies -7 volts dc; part of 46071.
3300-46119-1	Power supply assembly, dual,	Supplies 5 volts and 25 volts to the somc circuitry.
LM-E-5	Power supply, 5-volts, some PS1	Supplies 5 volts dc; part of 46119.
LM-EE-28	Power supply, 25-volt, some PS2	Adjusted to supply 25 volts dc; part of 46119.
3300-46163-1	Fuse panel	Provides overcurrent protection for somc power supplies.

Table 1-3. Equipment Supplied (Continued)

Nomenclature	Name	Function
3300-40015-1	Blower assembly, emi/rfi shield	Provides cooling air flow for somc cabinet.
3300-46120-1	Panel, electrical equipment, shield return	Provides mass single-point termination of shielding.
3300-46130-1	Panel, power distribution	Provides power distribution point for somc.

Table 1-4. Equipment Required But Not Supplied

Nomenclature	Name	Function
H33-5245M	Frequency counter	Converts frequency input to binary coded output; inputs from the matrix B, outputs to the signal data converter; externally controlled by the matrix multiplexer in the system control group.
H16-8405A	Vector voltmeter	Used to measure input voltage as well as phase relationships between two input probes; input is rf voltage, output is analog; externally controlled by the matrix multiplexer in the system control group.

1-8. Model Differences.

Differences in the monitor and test group exist between the V7 and V8 site equipment as a result of switch matrix size differences. The group C sampling matrices for the V7 site have 400 inputs and the V8 site group C matrices have 805 inputs. The switch matrix on the V7 site has two power supplies less than V8; therefore, there are two less power supply alarm indicators on the somc control panel. Also, there are fewer switch matrix temperature alarms. The special projects power supply alarm indicators on the V8 somc control panel are not included on the V7 somc panel. The switch matrix power supply fail indicators A1 and A2 (N6) are not included on the V7 somc panel.

1-9. Reference Designations. (See table 1-5 and figures 1-2 through 1-5.)

Reference designators are composed of rack numbers followed by area locations within the rack. A list of reference designators of given in table 1-5. Figures 1-2, 1-3, 1-4, and 1-5 are provided as a location guide to the reference designators.

Table 1-5. Reference Designations

Reference Designator (EQUIPMENT LOCATION)	Name	Reference Figure No.
411	Rfi test rack	1-2
412	Directional couplers rack	1-2
413	Matrix 2 rack	1-2
414	Matrix 1 rack	1-2
217	Console, Operation & Maintenance OJ-263/FLR-9(V) (somc, 3300-36005-1)	1-5
203	Jack panel	1-3, 1-4
204	Jack panel	1-3, 1-4
205	Jack panel	1-3, 1-4
411A1	Converter, Signal Data CV-2977/ FLR-9(V) (signal data converter 44051-1)	1-2
411A2	Vector voltmeter (vvm)	1-2
411A3	Divider Assembly Power Rf CU-2048/FLR-9(V) (power divider 3300-44096-1)	1-2
411A4	Analog-to-digital converter	1-2
411A5	Analog-to-digital converter	1-2
411A6	Frequency counter	1-2
412A1	Filter Assembly, Band Pass F-1339/ FLR-9(V) (bandpass filters band A, 3300-44093-1)	1-2

Table 1-5. Reference Designations

Reference Designator (EQUIPMENT LOCATION)	Name	Reference Figure No.
412A2	Filter Assembly, Band Pass F-1337/ FLR-9(V) (bandpass filters band B, 3300-44093-2)	1-2
412A3	Filter Assembly, Band Pass F-1338/ FLR-9(V) (bandpass filters band C, 3300-44093-3)	1-2
413A1	Generator, Signal SG-1003/FLR-9(V) (signal source band A, 3300-44038-1)	1-2
413A2	Generator, Signal SG-1002/FLR-9(V) (signal source band B, 3300-44038-2)	1-2
413A3	Generator, Signal SG-1001/FLR-9(V) (signal source band C, 3300-44038-3)	1-2
413A4A1	Band A matrices, group B	1-2
413A4A2	Band B matrices, group B	1-2
413A4A3	Band C matrices, group 8	1-2
413A4A4	Interface Unit, Digital MX-9250/ FLR-9(V) (digital interface unit 3300-44175-2) group B	1-2
414A1A1	Band A matrix, group A	1-2
414A1A2	Band B matrix, group A	1-2
414A1A3	Band B matrix, group A	1-2
414A1A4	Band C matrix, group A	1-2
414A1A5	Interface Unit, Digital MX-9251/ FLR-9(V) (digital interface unit 3300-44175-1), group A	1-2
414A2	Junction box, alarm	1-2
414A3	Power Supply PP-6811/FLR-9(V) (power supply No. 1, 3300-44100-1)	1-2
(V7) 203A11	Power Supply PP-6810/FLR-9(V) (power supply No. 2, 3300-44101-1)	1-3
(V7) 204A11	Matrix, group C	1-3

Table 1-5. Reference Designations (Continued)

Reference Designator (EQUIPMENT LOCATION)	Name	Reference Figure No.
(V7) 204A12	Interface Unit, Digital MX-9248/ FLR-9(V) (digital interface unit, 3300-44175-4) group C	1-3
(V7) 205A11	Matrix, group C	1-3
(V7) 205A12	Matrix, group C	1-3
(V8) 203A11	Power Supply PP-6814/FLR-9(V) (power supply No. 3, 3300-44102-1)	1-4
(V8) 204A11	Matrix, group C	1-4
(V8) 204A12	Matrix, group C	1-4
(V8) 204A13	Interface Unit, Digital MX-9247/ FLR-9(V) (digital interface unit, 3300-44175-3) group C	1-4
(V8) 205A11	Matrix, group C	1-4
(V8) 205A12	Matrix, group C	1-4
(V8) 205A13	Matrix, group C	1-4
(Front) 217A1	Panel, Switching SA-1873/FLR-9(V) [control panel, somc (V8), 3300-461701	1-5
217A1	Panel, Switching SA-1872/FLR-9(V) [control panel, somc (V7), 3300-46112-1]	1-5
217A2	Power distribution panel	1-5
217A3	Power Supply PP-6809/FLR-9(V) (power supply, -7 volts dc, 3300-46071-1)	1-5
217A4	Blower	1-5
(Rear) 217AB1	Shield return panel	1-5
217AB2	Controller, somc 3300-46050	1-5
217AB3	Power distribution panel	1-5
217AB4	Power supply, dual 3300-46119	1-5
217AB5	Panel, fuse	1-5

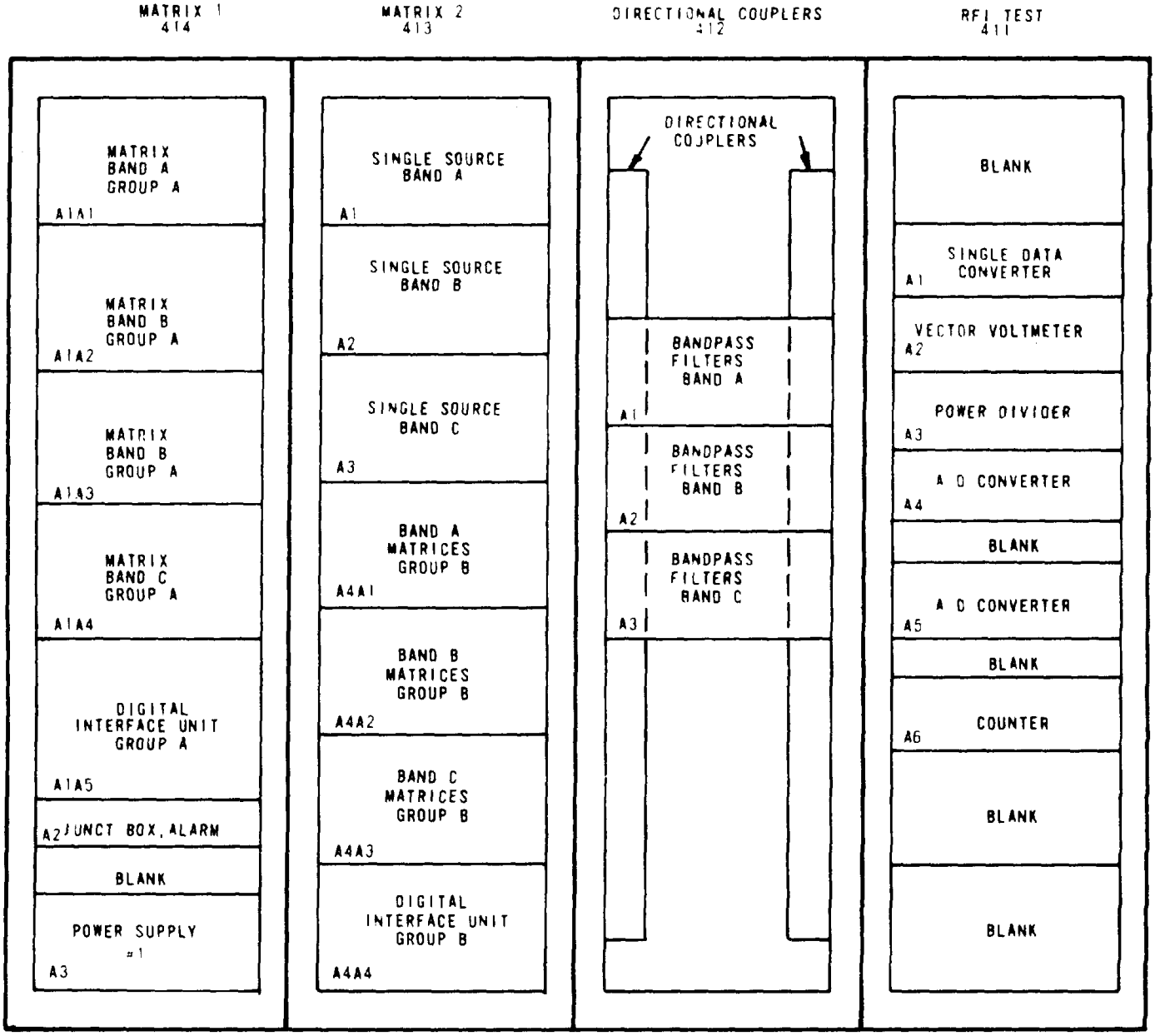

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Figure 1-2. Olm&t Subgroup Equipment Arrangement, Central Building, V7 and V8

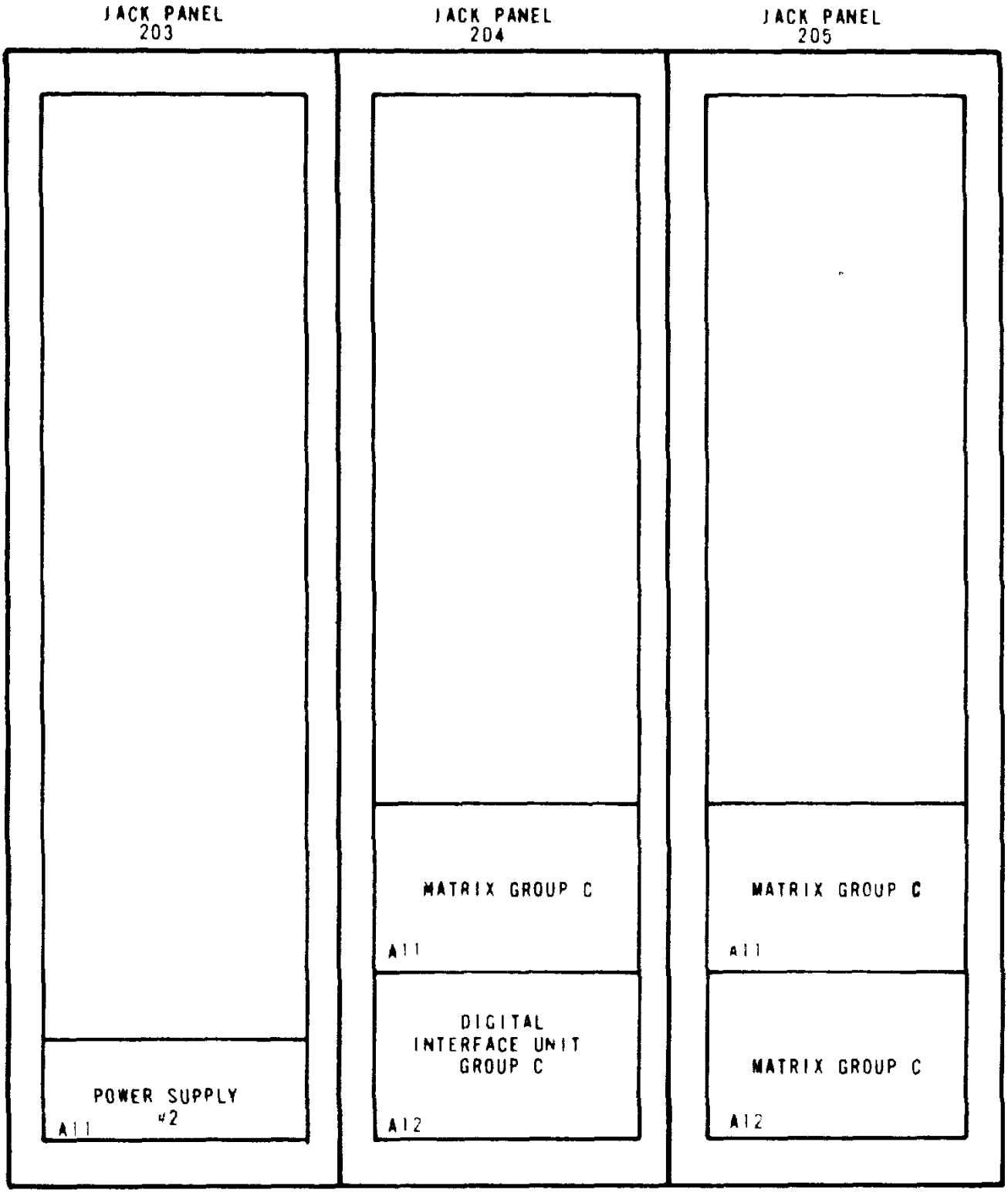


Figure 1-3. Olm&t Subgroup, C Matrix Equipment, Operations Building, V7

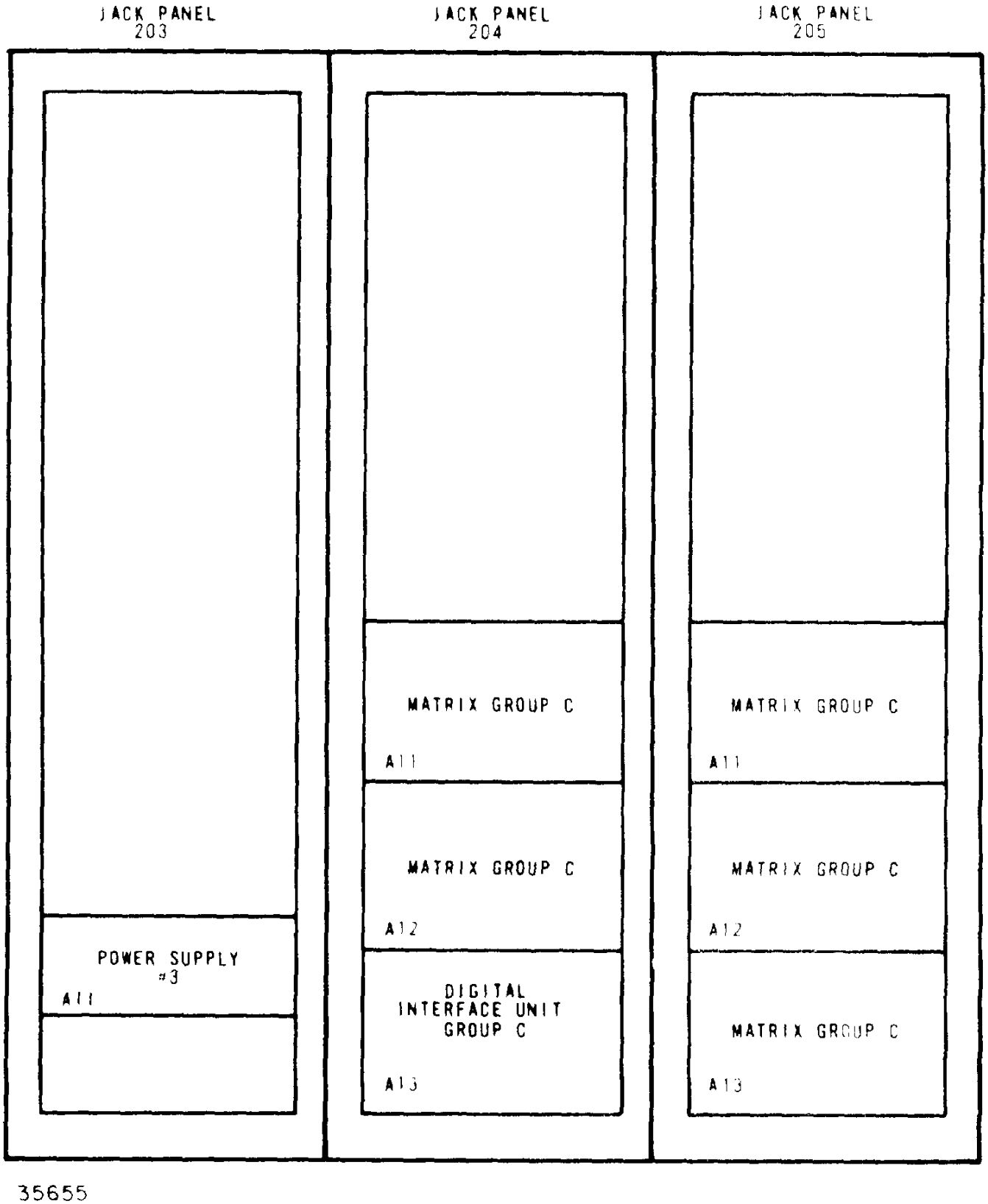


Figure 1-4. Olm&t Subgroup, C Matrix Equipment, Operations Building, V8

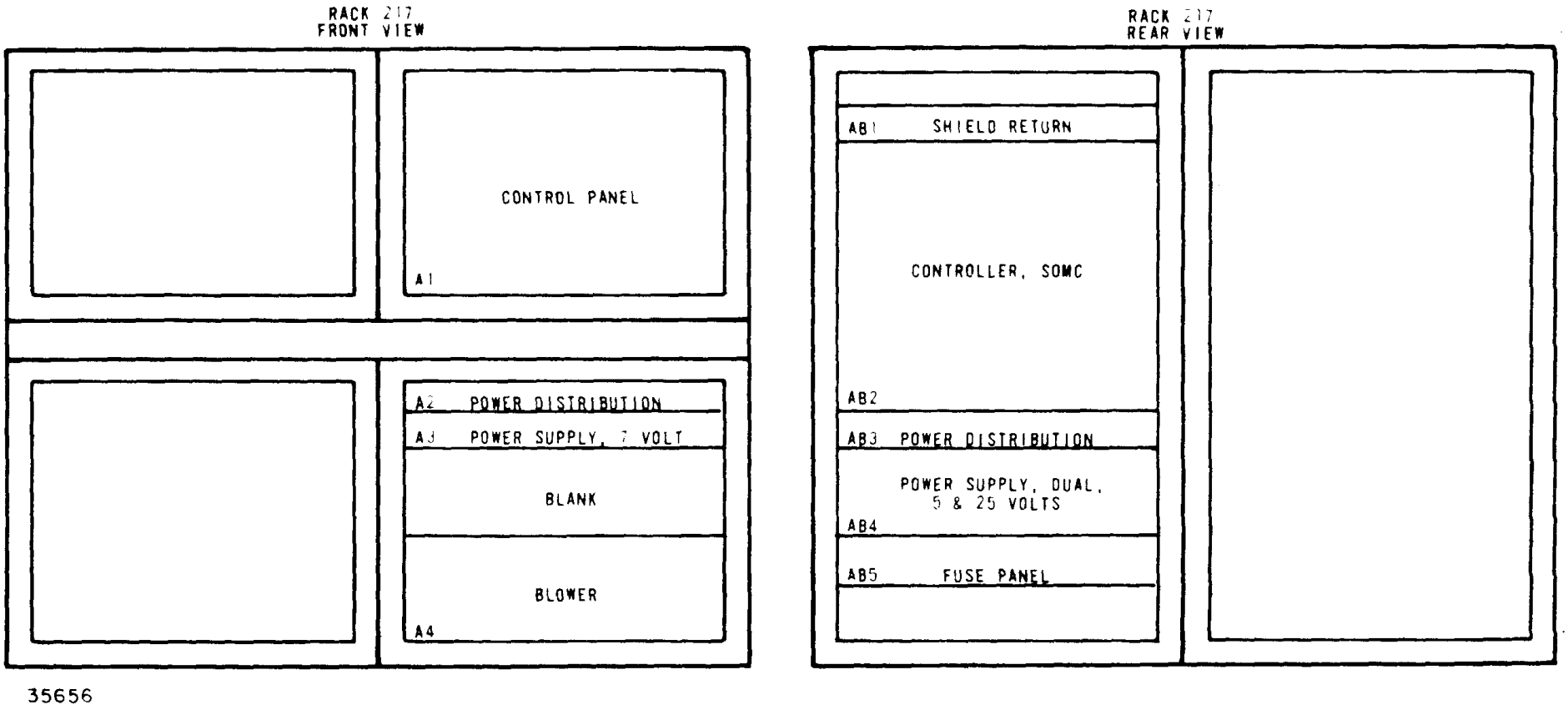


Figure 1-5. Monitor Subgroup, Somc Equipment, Operations Building, V7 and V8

1-10. List of Publications. (See table 1-6.)

A list of publications referenced in the monitor and test group instruction manual is given in table 1-6.

Table 1-6. List of Publications

Title	Publications No.
Set Manual, Countermeasures Receiving Set AN/FLR-9(V7)	IM 32-5895-231-15
Set Manual, Countermeasures Receiving Set AN/FLR-9(V8)	IM 32-5895-231-15/1
Hewlett-Packard Vector Voltmeter H16-8405A	CM 32-6625-240-14
Hewlett-Packard Counter H33-5245A	CM 32-6625-239-14
Reed Switch Matrices, Groups A, B, and C	CM 32-5895-237-14
Lambda Power Supplies, all models	CM 32-6130-204-14
Lambda Overvoltage Protectors, all models	CM 32-6130-209-14
Lambda Power Supplies, LMCC 5, 8, and 24	CM 32-6130-208-14
Lambda Power Supplies, LMEE 8, 24, and 28	CM 32-6130-210-14
Lambda Power Supplies, LMB 5, 8, and 24	CM 32-6130-211-14
Lambda Power Supply, LMD 8	CM 32-6130-212-14
Lambda Power Supply, LM258	CM 32-6130-213-14
Lambda Power Supply, LME 5	CM 32-6130-214-14
Preston Scientific A/D Converter	CM 32-5820-241-14
Card Repair Manual for Countermeasures Receiving Set AN/FLR-9(V7)/(V8)	IM 32-5895-239-15
Simulator Differential Signal SM-664/FLR-9(V)	IM 32-6625-264-14
Analyzer, Differential Signal Output TS-3287/FLR-9(V)	IM 32-6625-265-14
Simulator, Single-Ended Signal SM-665/FLR-9(V)	IM 32-6625-266-14

SECTION II

INSTALLATION

2-1. Scope.

This section contains unpacking, inspection, location, and installation instructions for equipment contained in the monitor and test group.

2-2. Unpacking.

Upon receipt of the equipment, carefully open the shipping containers. Check that the containers are upright. Do not drive sharp tools into seams. Inspect containers for signs of damage before dismantling. After opening containers, carefully remove contents. Before discarding the shipping containers, determine if they should be saved for future use.

2-3. Inspection. (See table 2-1.)

After the shipping containers have been unpacked, visually inspect the cabinets and all assemblies for defects listed in table 2-1. Repair or replace all defective items before placing unit in operation.

Table 2-1. Inspection

Item	Procedure
Chassis	Check for dented or bent frame.
Circuit cards	Check for loose circuit cards in mating jacks. Check circuit card holder for bent runners and loose circuit cards.
Connectors	Check for bent, broken, or missing pins; distorted barrels and damaged potting compound.
Controls	Check for damaged, loose, or missing knobs and for bent shafts.
Cables	Check for frayed or otherwise damaged cables.

2-4. Cables. (See Section IX)

Cables used in the installation of the monitor and test group equipment are listed by wire numbers in section IX which references the proper wire list. The wire list referenced contains cable destinations.

2-5. Equipment Floor Space.

Monitor and test group equipment is mounted in equipment racks. Refer to the AN/FLR-9(V8) Set Manual IM 32-5895-231-15/1 (see table 1-6) for rack floor space requirements. Refer to paragraph 1-9 in this manual for rack location and reference designators.

2-6. Installation.

Perform the following procedural steps to install the olm&t equipment in applicable cabinets if the equipment is not preassembled.

a. Carefully place the equipment in the cabinet from the front side.
b. Attach the equipment to the cabinet by installing the retaining screws through the front panel.
c. Connect the proper cables to the equipment. See the appropriate cabling block diagram in Section IX for cable distribution.
d. Connect the power cords to 115 volts ac.

2-7. Initial Adjustments. (See Sections III, and V.)

Refer to section III of this manual for operating control instructions. Refer to section V for maintenance instructions.

SECTION III
OPERATION

3-1. Scope.

The purpose of this section is to familiarize the operator with the controls and indicators and normal turn-on, operate, and turn-off procedures. Also given are emergency operating and emergency turn-off procedures.

3-2. Controls and Indicators.

The following material illustrates, describes, or references controls and indicators in the monitor and test group.

a. Somc Control Panel (V7, V8). (Reference figures 3-1 and 3-2, and table 3-1.) The following figures and table identify, locate, and describe the function of the controls and indicators on the somc control panel.

Table 3-1. Somc Control Panel

Index	Control or Indicator	Function
1	DAY OF YEAR/HOURS/MINUTES/ SECONDS	Time indication in numerical day of year, hour, minutes, and seconds; day of year incremented daily by tty through computer; time is incremented by the master clock.
2	(OLM&T POWER SUPPLY) OPS 203 5V	Alarm switch/indicator; indicates olm&t 5-volt power supply failure supplying the group C matrix in rack 203; upon failure, the indicator flashes red and the audible alarm sounds; press indicator to stop flashing; indicator remains illuminated until supply voltage is restored; press SILENCE ALARM (27) to silence audible alarm.
3	(OLM&T POWER SUPPLY) OPS 203 8V	Alarm switch/indicator; indicates failure of 8-volt power supply for olm&t group C matrix in rack 203; action same as index item 2.
4	(OLM&T POWER SUPPLY) OPS 203 24V	Alarm switch/indicator; indicates failure of 24-volt power supply for olm&t group C Matrix in rack 203; action same as index item 2.

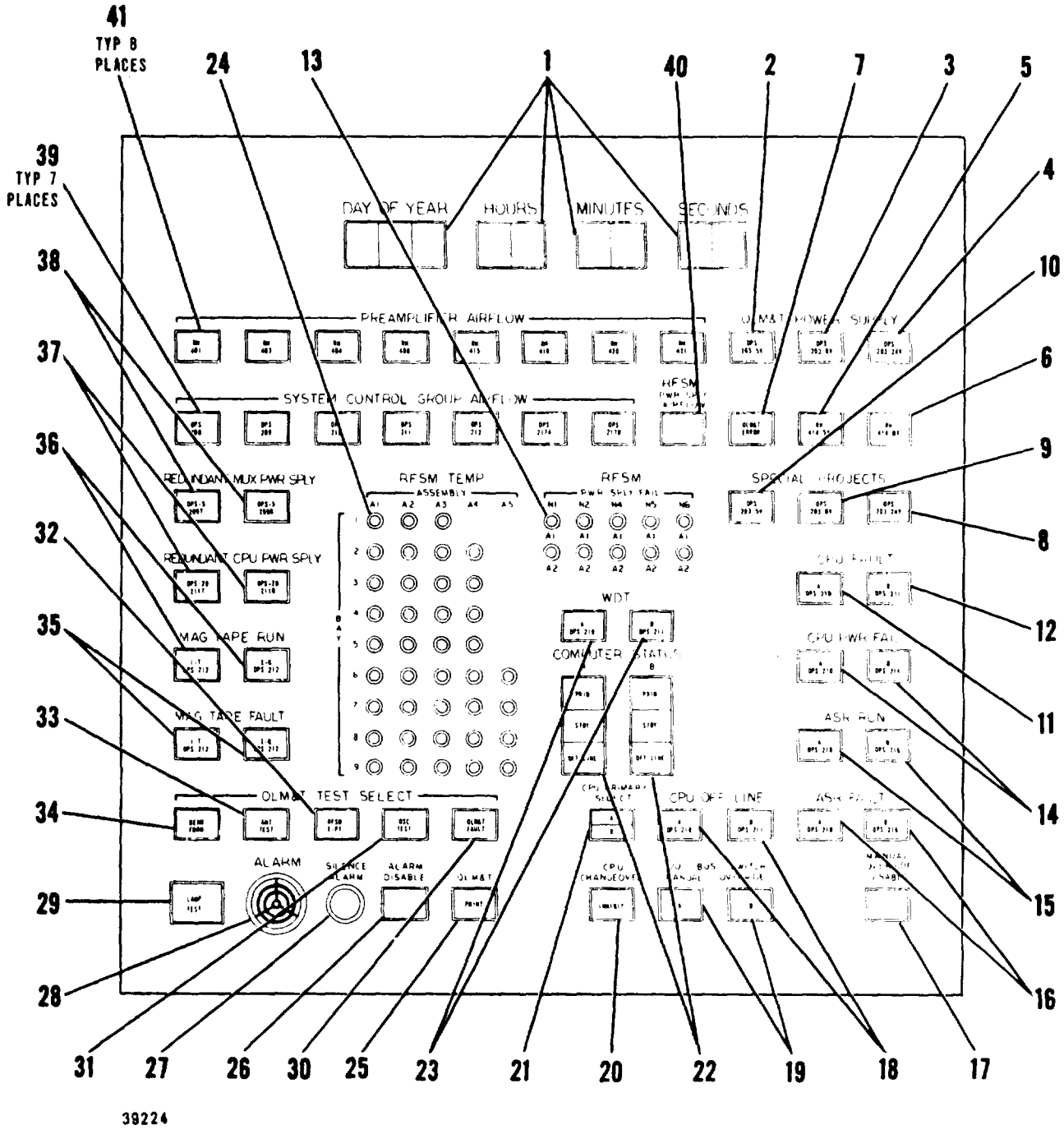


Figure 3-1. Controls and Indicators, Somc Control Pane. (V8)

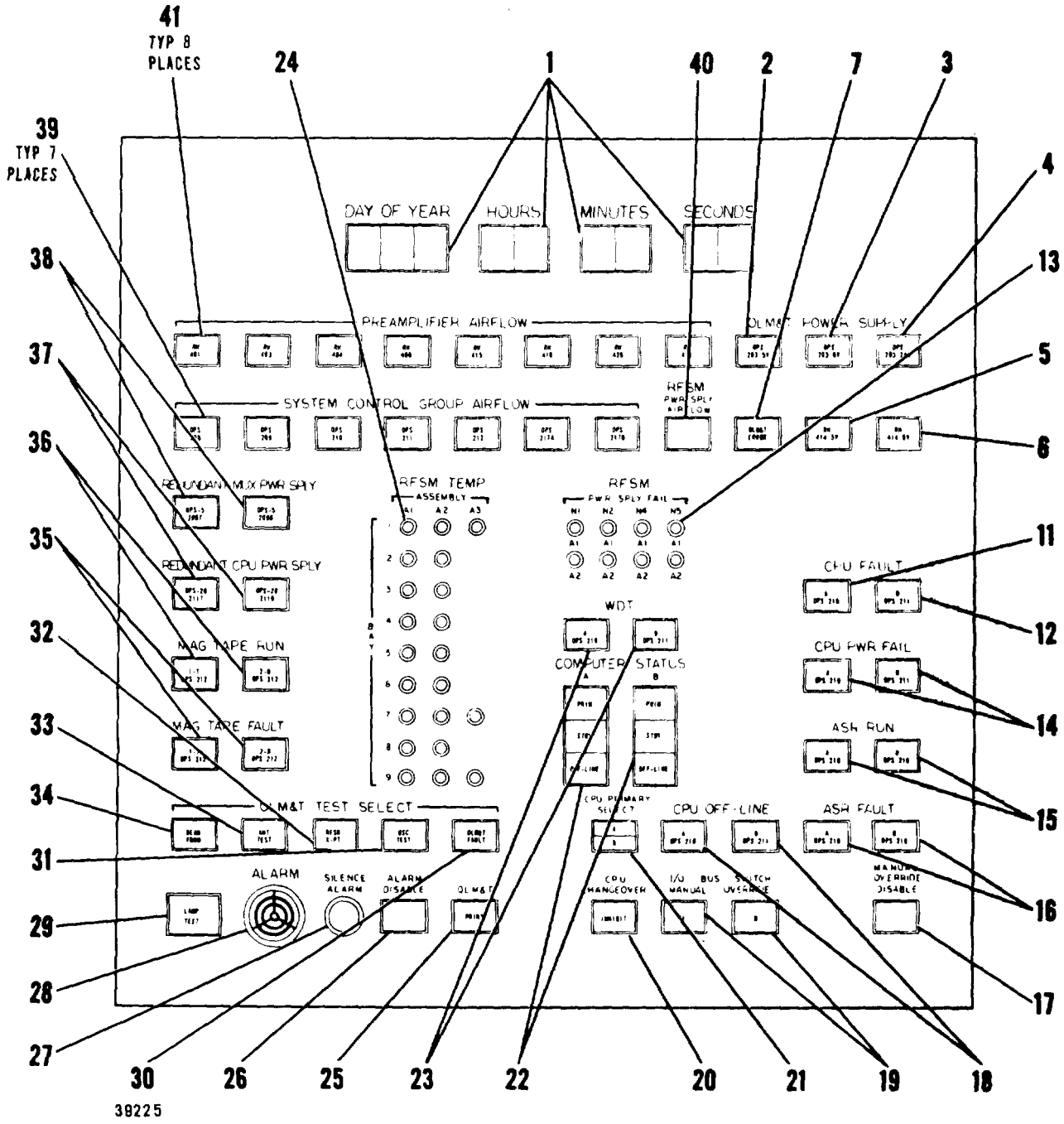


Figure 3-2. Controls and Indicators, Somc Control Pane. (V7)

Table 3-1. Somc Control Panel (Continued)

Index	Control or Indicator	Function
5	(OLM&T POWER SUPPLY) RH 414 5V	Alarm switch/indicator; indicates failure of 5-volt power supply for olm&t groups A and B matrices in rack 414; action same as index item 2.
6	(OLM&T POWER SUPPLY) RH 414 8V	Alarm switch/indicator; indicates failure of 8-volt power supply for olm&t groups A and B matrices in rack 414; action same as index item 2.
7	OLM&T ERROR	Status indicator; is illuminated yellow when index items 2, 3, 4, 5, or 6 alarms occur; computer is notified of olm&t malfunction and olm&t is ignored until alarm condition is cleared.
8 (V8 only)	(SPECIAL PROJECT) OPS 203 24V	Alarm switch/indicator; indicates failure of special project group 24-volt power supply in rack 203; action is same as index item 2.
9 (V8 only)	(SPECIAL PROJECT) OPS 203 8V	Alarm switch/indicator; indicates failure of special project group 8-volt power supply in rack 203; action same as index item 2.
10 (V8 only)	(SPECIAL PROJECT) OPS 203 5V	Alarm switch/indicator; indicates failure of special project group 5-volt power supply in rack 203; action same as index item 2.
11	(CPU FAULT) A OPS 210	Alarm switch/indicator; lights when a logic error is detected in the program; error is caused by hardware fault or illogical execution; alarm usually accompanied by CPU LOGIC ERROR or LOGIC ERROR, LEVEL N, ADDRESS $XXXX; message output to tty.
12	(CPU FAULT) B OPS 211	Same as index item 11.
13	(RFSM) PWR SPLY FAIL	Failure indicator; when lit red, indicates a switch matrix power supply Al or A2 failure in cabinets 219N1 through 219N6. Accompanied by audible alarm.

Table 3-1. Somc Control Panel (Continued)

Index	Control or Indicator	Function
14	(CPU PWR FAIL)	Alarm switch/indicator; controlled by computer assuming primary control; indicates computers A or B power failure; power failure causes indicator to flash red and audible alarm to sound; press indicator for steady illumination; press SILENCE ALARM to silence audible; indicator remains illuminated until multiplexer input signals return of power. NOTE If power failure occurs in primary computer, this action is preceded by a change of COMPUTER STATUS (22) unless computer changeover is inhibited.
15	(ASR RUN) OPS 218 B OPS 216	Status indicator; is illuminated green when the indicated tty is in a run condition.
16	(ASR FAULT) A OPS 218 B OPS 216	Fault indicator; lights when ASR controller circuit detects a timing error or a failure to acknowledge fault. Indicates status of controller, not units 216 and/or 218.
17	MANUAL OVERRIDE DISABLE	Control indicator; provides a momentary contact closure when pressed to remove the manual override condition established by index item 19; lamp lights white. Switch is covered to prevent accidental actuation.
18	(CPU OFF-LINE) A OPS 210 B OPS 211	Control indicator; used to take the standby computer off-line for maintenance purposes; if an attempt is made to take the primary computer off-line, the tty prints ILLEGAL SOMC INPUT; the indicator lights white and the switch is covered to prevent accidental actuation.
19	(1/O BUS SWITCH MANUAL OVERRIDE) A	Control/indicator; transfers the mission oriented hardware to the selected computer; overrides computer programmed selection; selected control/indicator is illuminated

Table 3-1. Somc Control Panel (Continued)

Index	Control or Indicator	Function
	(I/O BUS SWITCH MANUAL OVERRIDE) B	white when activated; switches are covered to prevent accidental actuation; control is cleared by pressing index item 17.
20	(CPU CHANGEOVER INHIBIT)	Control/indicator; inhibits automatic and manual computer changeover when activated; is illuminated white when activated; switch is covered to prevent accidental inhibit; switch is to be set when either computer is taken off-line.
21	(CPU PRIMARY SELECT) A B	Control/indicator; push to select a computer for primary status in a two-computer environment; the split screen is illuminated white to indicate which cpu was last selected; switches are covered to prevent accidental selection.
22	(COMPUTER STATUS) A PRIM STBY OFF-LINE B PRIM (green) STBY (yellow) OFF-LINE (red)	Light to indicate status of respective computer: PRIMARY indicates the computer is controlling system and is the computer designated to control the operating system. STBY indicates the computer is active, but is prepared to receive data from the primary computer via the intercomputer data channel only it is not controlling the system. OFF-LINE indicates the computer is not active, and is not ready to receive data from the primary computer and execute the operational program.
23	(WDT) A B	Alarm switch/indicator; indicates watchdog timer has overflowed, taking the computer (whose indicator is illuminated) off-line; if watchdog timer overflow occurs in primary computer, and if computer changeover is not inhibited, the standby computer becomes primary; action is the same as index item 2.
24	(RFSM TEMP) ASSEMBLY Al A2 A3 A4 A5 BAY 1 2 3 4 5 6 7 8 9	Indicators; indicate excessive temperature in an area of the switch matrix identified by the assembly and bay number of the illuminated indicator; audible alarm sounds when this occurs; press the SILENCE ALARM (27) control to silence; alarm is illuminated red until trouble is corrected.

Table 3-1. Somc Control Panel (Continued)

Index	Control or Indicator	Function
25	(OLM&T) PRINT	Control/indicator; when set, all test results are typed out on the tty; illuminated white when set; press again to reset.
26	ALARM DISABLE	Control/indicator; press to disable audible alarm; illuminated white when activated; press again to restore; switch covered to prevent accidental disable.
27	SILENCE ALARM	Control; press to reset audible alarm circuit and silence alarm; momentary switch.
28	ALARM	Audible alarm; sounds when activated; silenced by the SILENCE ALARM (27) or the ALARM DISABLE (26).
29	LAMP TEST	Control; press to test all somc control panel lamps. NOTE Audible alarm sounds when LAMP TEST is activated. (See index item 28.)
30	(OLM&T TEST SELECT) OLM&T FAULT	Press to disable the olm&t function (lamp lights white); tests described in index items 31 through 34 are suspended when switch is set; press again to continue the olm&t function; tests in progress resume at the point of interruption. CAUTION Switch paths are made without verification when switch is set (lamp lighted).
31	(OLM&T TEST SELECT) OSC TEST	Control/indicator; press to request oscillator test routine; tty acknowledges; illuminated white when activated; test repeats until switch is reset.
32	(OLM&T TEST SELECT) RFSM X-PT	Control/indicator; press to request switch matrix crosspoint test routine; tty acknowledges; illuminated white when activated; test repeats until switch is reset.

Table 3-1. Somc Control Panel (Continued)

Index	Control or Indicator	Function
33	(OLM&T TEST SELECT) ANT TEST	Control/indicator; press to request antenna continuity test routine; tty acknowledges; illuminated white when activated; test repeats until switch is reset.
34	(OLM&T TEST SELECT) BEAMFORM	Control/indicator; press to request beam-former test routine; tty acknowledges; illuminated white when activated; test repeats until switch is reset.
35	(MAG TAPE FAULT) I-T OPS 212 2-B OPS 212	Fault indicator; illuminated indicator (red) corresponding to the tape unit that has experienced a fault; audible alarm sounds when fault is sensed; tty outputs fault message.
36	(MAG TAPE RUN) I-T OPS 212 2-B OPS 212	Indicator; illuminated green when the tape unit corresponding to the indicator is in a run condition.
37	(REDUNDANT CPU PWR SPLY) OPS-28 211T OPS-28 211B	Alarm indicators; illuminated red with audible alarm when either of the redundant +28-volt power supplies fail.
38	(REDUNDANT MUX PWR SPLY) OPS-5 209T OPS-5 209B	Alarm indicator; indicator is illuminated red with audible alarm when either of the redundant multiplexer power supplies fail.
39	(SYSTEM CONTROL GROUP AIRFLOW) OPS 208 OPS 209 OPS 210 OPS 211 OPS 212 OPS 217A OPS 217B	Alarm switch/indicator; flashes red when airflow in the unit location indicated falls below a set amount; audible alarm sounds, press for steady red illumination; indicator is extinguished when airflow resumes.
40	RFSM PWR SPLY AIRFLOW	Air flow indicator; action same as index item 39 when any of the six power supply cabinets lose airflow.
41	(PREAMPLIFIER AIRFLOW) RH 401 RH 403 RH 404 RH 408 RH 415 RH 416 RH 420 RH 421	Alarm switch/indicator; action same as index item 39 for indicated unit location.

b. Signal Source Panel. (Reference figure 3-3.) The signal source panel shown in figure 3-3 is typical of bands A, B, and C signal source attenuator controls. One control is provided for each of the six oscillators in the assembly. Adjustment of these attenuators is a maintenance calibration. Refer to section V (Maintenance and Repair) for adjustment procedure. At the rear of each unit is the POWER switch Setting the switch to the ON position activates the signal source panel.

Figure 3-3. Controls and Indicators, Typical Signal Sources Assembly

c. Signal Data Converter. (Reference figure 3-4.) The attenuator control shown in figure 3-4 is an input level adjustment to the vector voltmeter and frequency counter. Adjustment of this control is described in section V (Maintenance and Repair). At the rear of the unit is the POWER switch. Setting the switch to the ON position activates the signal data converter.

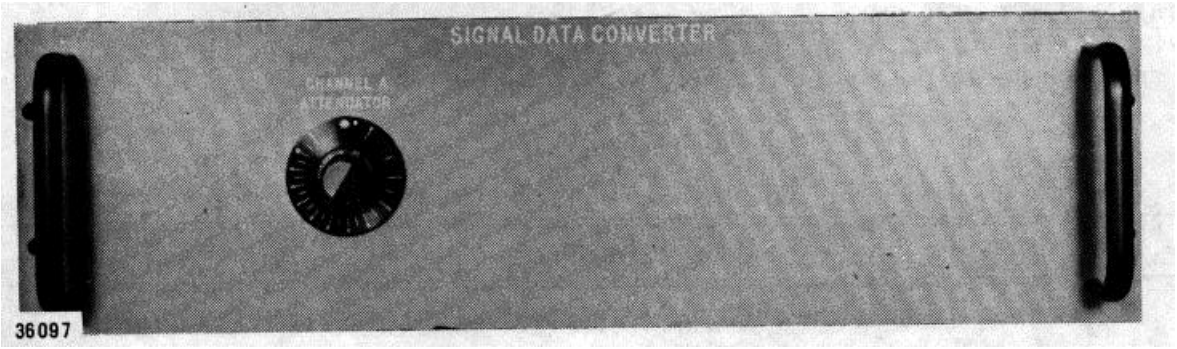


Figure 3-4. Controls and Indicators, Signal Data Converter

d. Vector Voltmeter. Location and description of the vector voltmeter controls and indicators are found in the manufacturer's manual as listed in table 1-6, section 1.

e. A/d Converters. Location and description of the controls and indicators on the a/d converters are found in the manufacturer's manual as listed in table 1-6, section 1.

f. Monitor and Test Group Power Supplies. (See figure 3-5.) There are no indicators in the monitor and test group power supplies. Shown in figure 3-5 is the rear of a typical power supply, showing the ac power switch. Setting the switch to the ON position activates the power supply.

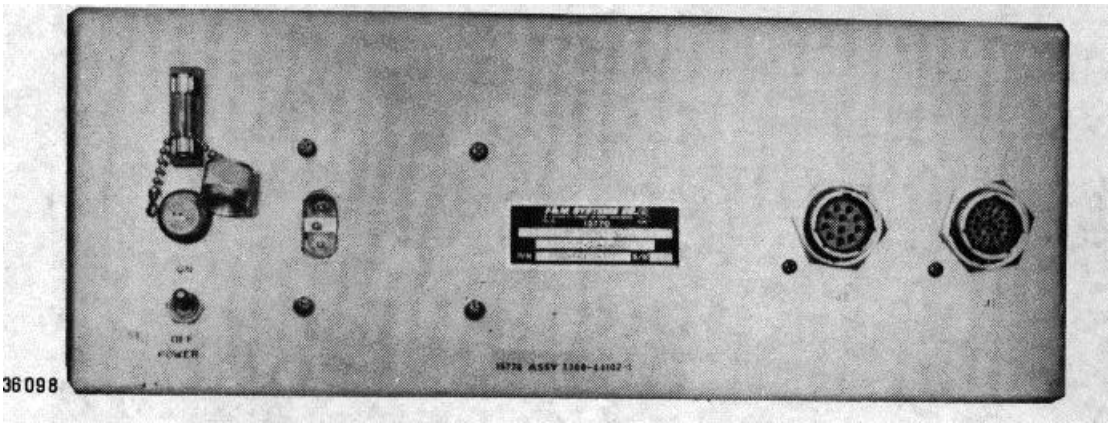


Figure 3-5. Controls and Indicators, Typical Power Supply, Rear View

3-3. Monitor and Test Group Turn-On Procedures.

a. Application of Main Power. The application of main power to the monitor and test group equipment consists of activating the circuit breakers for each equipment. In the central building, olm&t primary power is applied to cabinets 411, 412, 413, and 414 from an appropriately labeled circuit breaker. In the operations building, primary power is applied to the olm&t group C matrix, power supply and the jack panel racks from a circuit breaker mounted above the racks. The somc is energized by a circuit breaker mounted above the equipment.

b. Initialization of Monitor and Test Group Equipment. (See tables 3-2, 3-3, and 3-4.) Continue to apply power to the monitor and test equipment using the turn-on procedures defined in tables 3-2, 3-3, and 3-4.

Table 3-2. Turn-On Procedure for Olm&t Consoles

Step	Procedure
1	At cabinet 411, vector voltmeter, ensure that the CHANNEL SELECT switch is set to the PROGRAM position and that the POWER switch is set on ON. Set phase METER OFFSET to 180 degrees.

Table 3-2. Turn-On Procedure for Olm&t Consoles (Continued)

Step	Procedure
2	At cabinet 411, frequency counter, ensure that the FUNCTION switch is set to FREQUENCY. Ensure that the SAMPLING RATE control is rotated clockwise from the POWER OFF position. Ensure that TIME BASE is set to 1 second. Ensure that SENSITIVITY is set to PLUG IN.
3	At cabinet 411, a/d converters, ensure that the ADC TRIGGER selector is in the NORMAL position and that the MODE switch is in the NORMAL position.
4	At the rear of cabinet 411, a/d converters, set the AC POWER switch on each unit to ON.
5	Cabinet 412 has no power switching, proceed to cabinet 413.
6	At the rear of cabinet 413, set the AC POWER switches of the three oscillator units to ON.
7	At the rear of cabinet 414, set the AC POWER switch of the power supply to ON.

Table 3-3. Turn-On Procedure for Group C Matrix

Step	Procedure
1	In the operations building, lower portion of the jack panel racks 203, 204, and 205, locate the group C matrix.
2	At the rear of the power supply, rack 203, open the equipment door and ensure that the AC POWER switch is on.

Table 3-4. Turn-On Procedure for Somc Console 217

Step	Procedure
1	Set the main power circuit breaker to ON.
2	On the some control panel, press the LAMP TEST switch and determine that all indicating lamps are operational.
3	Actuate the ALARM DISABLE switch until all equipment in the system has been energized and brought to normal operating status.
4	Reset the ALARM DISABLE switch to allow audible alarm to sound when an alarm occurs.
5	Inspect all alarm lamps to determine that there are no hardware alarms. Correct any malfunctions before proceeding.

3-4. Monitor and Test Group Operating Procedures.

a. System Startup. Place the system in operating condition according to procedures in the Set Manual (see table 1-6).

b. Operating the Olm&t Test Select Controls. (See table 3-5.) To select one of the four olm&t routines from the somc panel, proceed as described in table 3-5. Note that when more than one test select control is set the tests selected will be performed in the following order: beamformer, antenna, switch matrix oscillator. These selected tests will continually sequence in this order until controls are reset.

Table 3-5. Olm&t Test Select Controls Operation

Step	Procedure
1	If the complete test results are to be typed on the tty, set the OLM&T PRINT control. The control is illuminated when set.
2	Set OLM&T TEST SELECT CONTROLS. The control is illuminated when set. Note that the test will be repeated until the control is reset.
3	The test program outputs OLMT X TEST START. The time and date are then output to record the time and date of test. The X is the name of the test to be performed where OSC is oscillator test, BMFR is beamformer test, ANT is antenna test, and RFSM is switch matrix test.

Table 3-5. Olm&t Test Select Controls Operation (Continued)

Step	Procedure
4	If a test result is out of tolerance, the computer outputs fault messages as shown in table 5-3.
5	After completing the test, the computer outputs OLMT X TEST FINISHED, with X being the same as described in step 3.
6	After completion of the olm&t test, the operator resets the OLM&T select control, extinguishing it and halting the test.
7	Olm&t test cycling is halted and further olm&t test requests ignored if the OLM&T FAULT control is set (illuminated if set). Olm&t tests continue where halted when OLM&T FAULT control is reset.
8	Reset the OLM&T PRINT control to OFF if previously set.

c. Tty Control of the Monitor and Test Function. The tty associated with each computer provides system testing beyond the four olm&t test routines on the somc control panel. To request additional tests, the appropriate request format is typed on the tty keyboard servicing the current primary computer. The tty inputs all have the same basic format consisting of a command followed by a carriage return. The carriage return signals a completed command. Correct typographical errors by using the / (slash) key and repeating the entire request. If a command is formatted incorrectly, the computer outputs ILLEGAL FORMAT. If the command is formatted correctly, the computer outputs the day and time and executes the command. Consult the appropriate set manual (see table 1-6) for complete format instructions. Before typing a command, check the following items.

1. Scan the somc control panel to determine if the system is ready to receive a command.
2. Check the appropriate ASR RUN indicator to determine if the tty is ready.

CAUTION

Never use the standby tty to input commands or requests to the computer unless specifically called out in procedure. To do so may disrupt operation of standby computer.

3. With the ASR MODE switch in the K position, type the appropriate command.

d. Test Oscillator Selection. (See table 4-1.) For each frequency band, one of the six reference oscillators may be selected. The format for this selection is: OSCILLATOR XX, or OSC XX, followed by a carriage return, where XX is the oscillator number.

Oscillators i through 6 serve band A; 7 through 12 serve band B; and 13 through 18 serve band C.

e. Individual Tests. Individual beamformers and specific switchpoints can be tested by entering the appropriate command given in set manual procedures.

3-5. Monitor and Test Group Turn-Off Procedures.

Individual rack-mounted units having a standard three-prong line cord and/or a power switch may be individually deenergized by unplugging the unit or by turning the POWER switch to OFF. Equipment racks or consoles for the monitor and test group are deenergized by opening the circuit breaker servicing that equipment (refer to paragraph 3-3).

3-6. Emergency Turn-Off Procedure.

Turn off the circuit breaker servicing the equipment(s) to be deenergized.

3-7. Emergency Operation.

Should the olm&t equipment fail, activate the OLM&T FAULT control. The olm&t functions are then ignored by the computer.

SECTION IV

THEORY OF OPERATION

4-1. Scope.

This section contains a description of the functional operation of the AN/FLR-9(V')/ (V8) monitor and test group. The content-is designed to aid maintenance personnel in understanding group and subgroup equipment operation and relationship to the remaining AN/FLR-9(V7) and (V8) groups.

4-2. Monitor and Test Group. (See figure 4-1.)

a. Functional Description. The monitor and test group performs monitoring and test functions for the other AN/FLR-9 functional groups. Monitor functions performed are equipment malfunction alarms, status indications, and performance reports. Voltage, phase, and frequency measurements are made as part of the following tests:

- Antenna test
- Switch matrix test
- Oscillator test
- Beamformer test

The monitor and test group hardware consists of four equipment racks in the central building, the Console, Operation and Maintenance OJ-263/FLR-9(V) (somc), and part of three equipment racks shared with the antenna group in the operations building. This group operates through the antenna and matrix groups to perform path verification and maintenance testing functions. Rf amplifiers and beamformers are checked through adjacent beam paths in the antenna group. These operations are controlled by the on-line computer through the system control group. Monitoring is accomplished through the somc. Reports and test results are received through the tty that is shared with the system control group. Part of the somc panel area is also shared with the system control group.

b. Control and Data Interface. (See figure 4-2 and tables 4-1, 4-2, and 4-3.) The monitor and test group is controlled by the output of the matrix multiplexer in the system control group. Data from the monitor and test group is routed to the cable scanner of the system control group. The cable scanner and matrix multiplexer are controlled by the primary computer.

1. Reed Switch Matrix Control. Control of the reed switch matrices is routed to the digital interface unit of each matrix from the matrix multiplexer. Control word format is given in table 4-1.

2. Vector Voltmeter Control. (See figure 7-6.) Control of vector voltmeter (vvm) phase and ranging is supplied by a cable from the matrix multiplexer and is routed through the decoding function in the signal data converter to the vvm.

3. Frequency Data Output. Output of the frequency counter is routed through the signal data converter line drivers to the cable scanner through two cables as a high order word and a low order word.

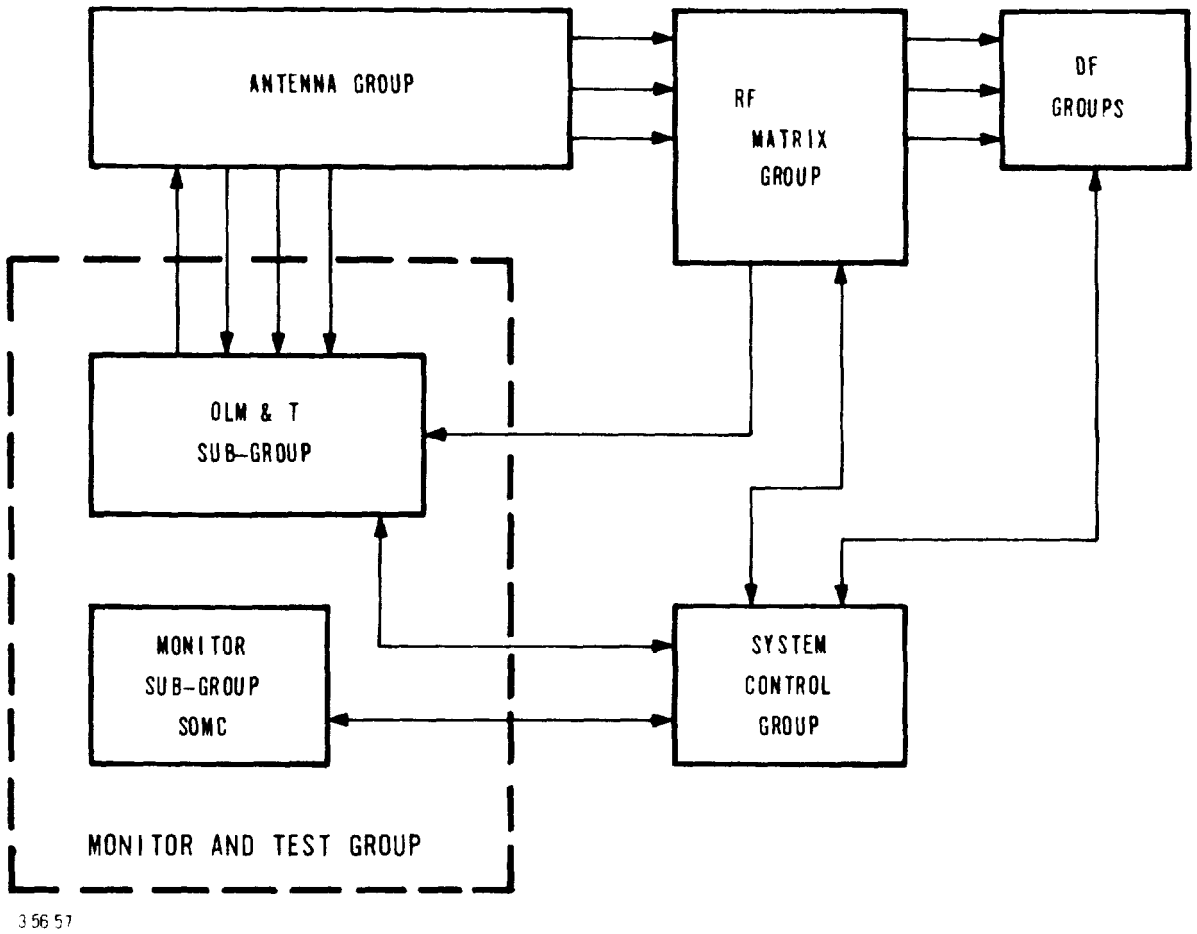


Figure 4-1. Monitor and Test Group System Interplay

4. Vector Voltmeter Output. Output of the vvm is through the a/d converters. One output cable supplies the vvm phase word to the cable scanner and one output cable supplies the vvm amplitude word. Output formats are given in table 4-3.

4-3. Olm&t Subgroup. (See figure 4-3 and 7-5.)

a. General. The monitor and test group functions as a test facility for the antenna group beamformers, the switching matrix, and the antenna elements. Selected oscillator signals are coupled through the group circuitry under test to the measuring equipment.

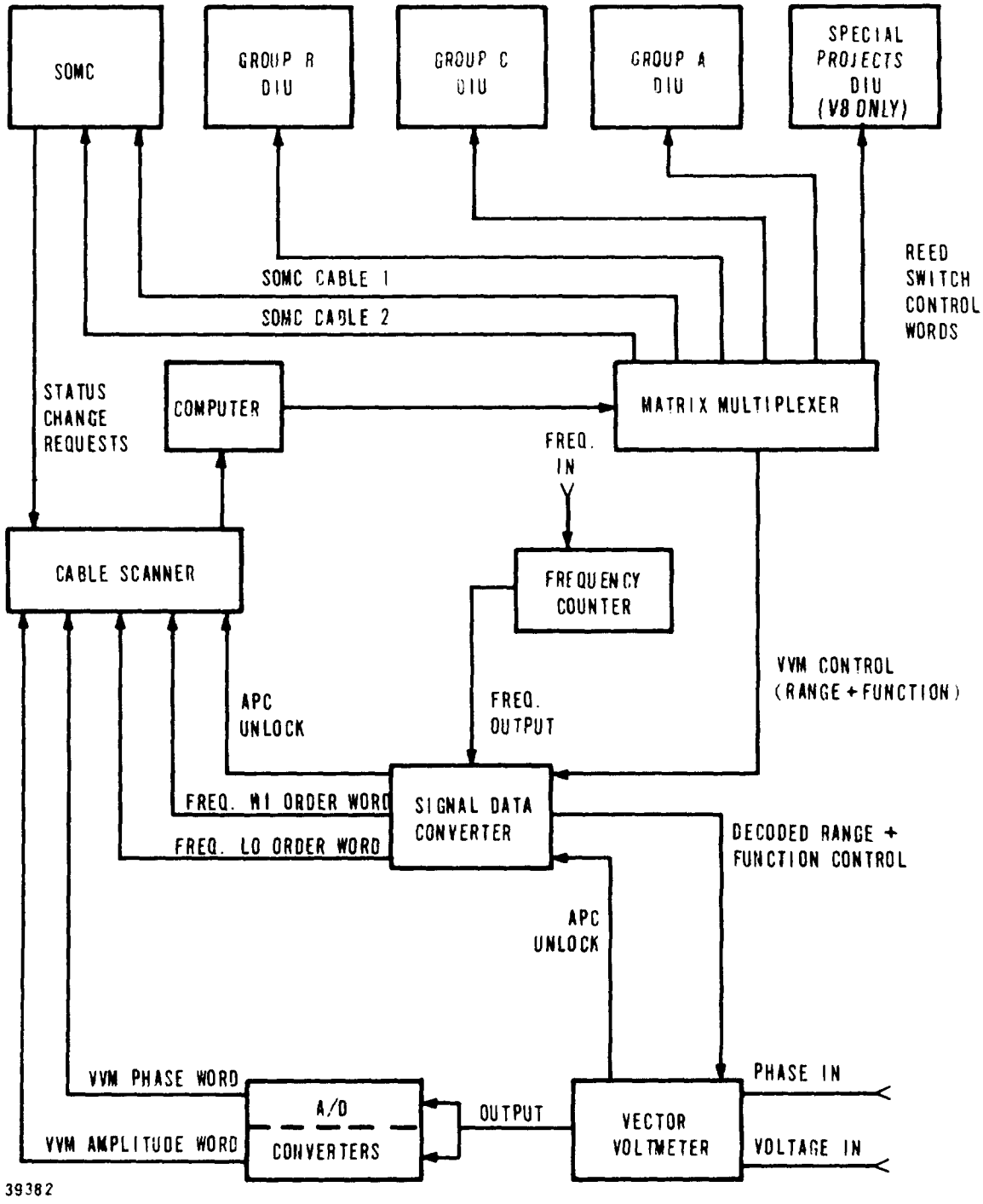


Figure 4-2. Control Diagram for Monitor and Test Components

Table 4-1. Reed Switch Matrices, Digital Input Format

Bit	Group A	Group B	Group C	Special Projects
0	Strobe (Not Used)	Strobe (Not Used)	Strobe (Not Used)	Strobe (Not Used)
1	Band A select	Band A select	Spare	Spare
2	Band B select	Band B select	Spare	Spare
3	Band C select	Band C select	Spare	Spare
4	1 = Antenna 0 = Beamformer	1 = PD3 0 = PD4	BCD (800)	Spare
5	Oscillator Select (4)	Filter Select (4)	BCD (400)	Spare
6	Oscillator Select (2)	Filter Select (2)	BCD (200)	Output Select (4)
7	Oscillator Select (1)	Filter Select (1)	BCD (100)	Output Select (2)
8	Channel No. (80)	Channel No. (80)	BCD (80)	Output Select (I)
9	Channel No. (40)	Channel No. (40)	BCD (40)	1 = Connect no input to selected output 0 = Connect selected input to selected output
10	Channel No. (20)	Channel No. (20)	BCD (20)	Input Select (32)
11	Channel No. (10)	Channel No. (10)	BCD (10)	Input Select (16)
12	Channel No. (8)	Channel No. (8)	BCD (8)	Input Select (8)
13	Channel No. (4)	Channel No. (4)	BCD (4)	Input Select (4)
14	Channel No. (2)	Channel No. (2)	BCD (2)	Input Select (2)
15	Channel No. (1)	Channel No. (1)	BCD (1)	Input Select (1)

Table 4-2. Signal Data Converter Frequency Output

High Order Word				Low Order Word			
Plug	**Pins**	**Word Bits**	**Decode**	**Plug**	**Pins**	**Word Bits**	**Decode**
J3	A & B	BCD 1	Digit 1	J4	A & B	BCD 1	Digit 5
	D & E	BCD 2			D & E	BCD 2	
	G & H	BCD 3			G & H	BCD 3	
	K & L	BCD 4			K & L	BCD 4	
J3	P & N	BCD 1	Digit 2	J4	P & N	BCD I	Digit 6
	S & T	BCD 2			S & T	BCD 2	
	W & V	BCD 3			W & V	BCD 3	
	Y & Z	BCD 4			Y & Z	BCD 4	
J3	b & c	BCD 1	Digit 3	J4	b & c	BCD 1	Digit 7
	e & f	BCD 2			e & f	BCD 2	
	h & i	BCD 3			h & i	BCD 3	
	k & m	BCD 4			k & m	BCD 4	

Table 4-2. Signal Data Converter Frequency Output (Continued)

High Order Word				Low Order Word			
Plug	Pins	Word Bits	Decode	Plug	Pins	Word Bits	Decode
J3 p & q s & t v & w y & z	BCD 1 BCD 2 BCD 3 BCD 4	Digit 4	J4	p & q s & t v & w y & z	BCD 1 BCD 2 BCD 3 BCD 4	Digit 8	

Table 4-3. A/d Converter Control Inputs And Outputs

Pin	Function	Pin	Function
A	No connection	a	Shield
B	No connection	b	Data Bit 128 (Complement)
C	No connection	c	Data Bit 128
D	Start Command (High)	d	Shield
E	Start Command (Low)	e	Data Bit 64 (Complement)
F	Shield	f	Data Bit 64
G	No connection	g	Shield
H	No connection	h	Data Bit 32 (Complement)
J	No connection	i	Data Bit 32
K	End Of Conversion (Complement)	j	Shield
L	End Of Conversion	k	Data Bit 16 (Complement)
M	Shield	m	Data Bit 16
N	Data Bit 2048 (Complement)	n	Shield
P	Data Bit 2048	p	Data Bit 8 (Complement)
R	Shield	q	Data Bit 8
S	Data Bit 1024 (Complement)	r	Shield
T	Data Bit 1024	s	Data Bit 4 (Complement)
U	Shield	t	Data Bit 4
V	Data Bit 512 (Complement)	u	Shield
W	Data Bit 512	v	Data Bit 2 (Complement)
X	Shield	w	Data Bit 2
Y	Data Bit 256 (Complement)	x	Shield
Z	Data Bit 256	y	Data Bit 1 (Complement)
z	Data Bit 1		
aa	Shield		

NOTE

This format is the same for both the amplitude word and the phase word. Connector J2 is used on each converter.

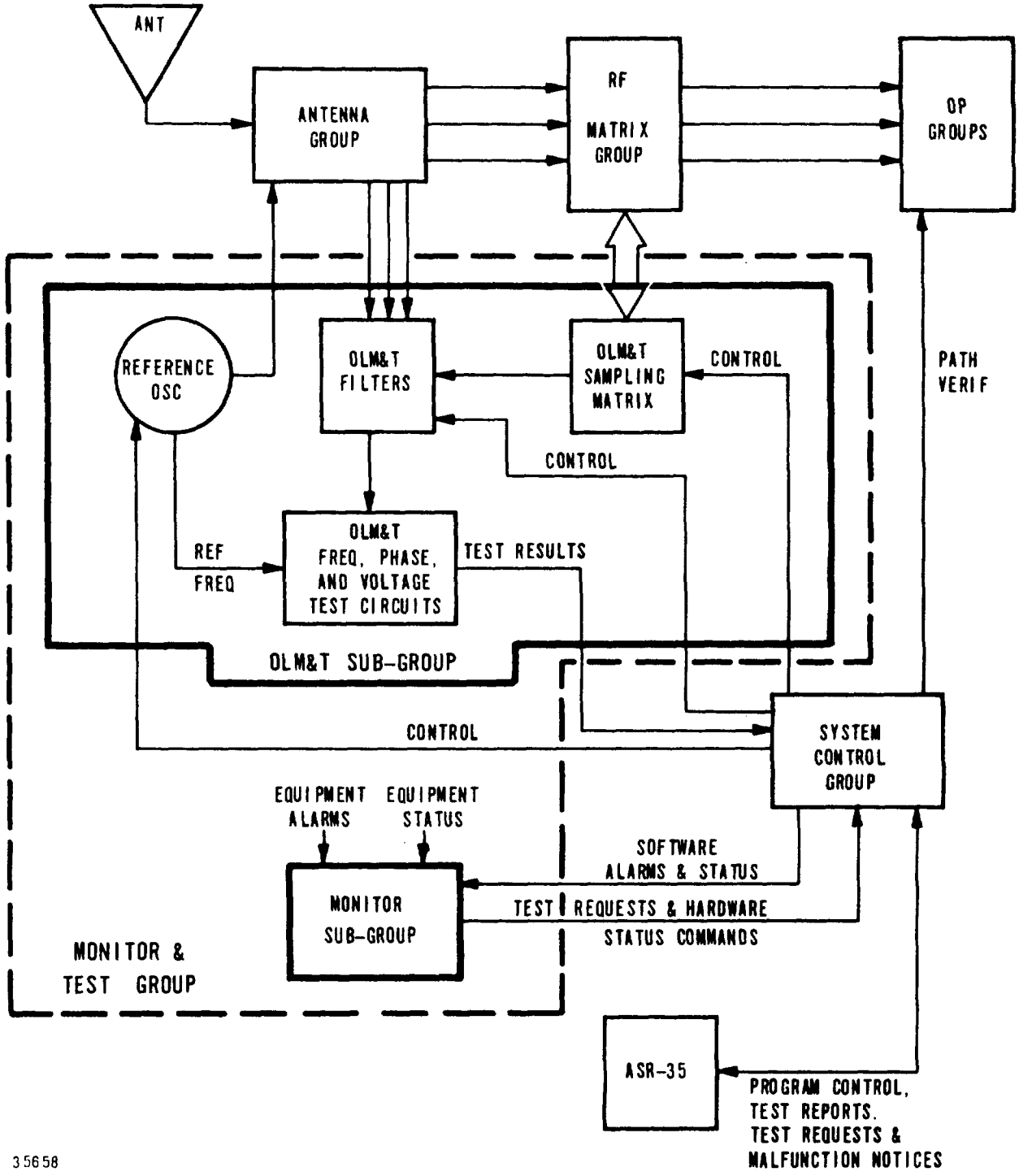


Figure 4-3. Monitor and Test, Subgroup Interplay

The same selected oscillator signal is also coupled directly to the measuring equipment. The olm&t measuring equipment, upon receiving the two signals, measures amplitude or frequency or compares them for any differences in phase. The test parameters are coupled to the computer and if found to be within limits, the tested circuitry is assumed to be functioning correctly.

b. Olm&t Cable Test. (See figure 7-5.) The cable test is a preliminary check in the beamformer test routine to insure that the olm&t oscillators, matrices, and measuring equipment are operating properly. Amplitude and phase readings are taken from each of the three selected oscillators through a test cable path to the measuring equipment. These readings are compared with reference values stored in computer memory. A cable test is made for each of the three bands. Using band B as an example, refer to sheet 2 of figure 7-5. Observe that olm&t oscillators 7 through 12 may be selected and routed through matrix AIB, A2B, and A3B2 to output port 99 (test cable). The test cable is connected to the unused filter number of input position of filter output matrix B3B. The output of this matrix (test signal, band B) is connected to the 3-to-1 power combiner PD2. The reference signal (oscillator reference output, band B) is applied to PDI, and hence to the vector voltmeter for amplitude and phase measurements.

c. Interference Test. (See figure 7-5.) In the interference test for a specified band the omni beamformer is connected through the olm&t filter corresponding to the selected test oscillator frequency to the vector voltmeter to be measured for amplitude. Note that the test oscillator output is not used in this test. If the amplitude is excessive, it is assumed that an interfering signal at the same frequency of the oscillator is being received by the antenna group. An interference test is made for the selected test oscillator frequency in each of the three bands. Using band B as an example, refer to sheet 2 of figure 7-5. Observe that the omni beamformer output is selected by the matrix B1B and passed through the olm&t filter for that frequency. The filter output is selected by the appropriate frequency select filter path and applied to the vector voltmeter through PD2 and PD3. If the measured amplitude exceeds the interference level amplitude value stored in the computer memory, the test oscillator selection will be incremented by one and the interference test repeated. This procedure is repeated until an oscillator frequency is found without excessive interference. If all six oscillators in a band, in this case oscillators 7 through 12, have excessive interference the originally selected oscillator will be used for olm&t testing.

d. Beamformer Test. (See figure 7-5.) Due to similarity, only the band A circuit is described. The beamformer and element test matrix (A1A and A2A) applies the oscillator signal through a directional coupler to a selected rf amplifier input line. The oscillator signal applied to the selected amplifier input line is coupled through the antenna group divider to the sector beamformer, omni beamformer, or monitor beamformer. Directional couplers at the output of the beamformers couple the oscillator signal to the beamformer test output matrix BIA. The test output matrix is commanded by the computer to select the directional coupler associated with the beamformer under test. The oscillator signal is coupled from the test output matrix to a selected bandpass filter between the filter select matrix (B2A) and the frequency select matrix (B3A). The bandpass filter rejects all but the selected oscillator frequency and the signal is coupled through the frequency select matrix to the power combiner PD2. The power combiner accepts signals from the band in test, either bands A, B, or C. The output of the power combiner PD2 is coupled to the power divider PD3 where the oscillator signal is divided into two signal channels of

equal amplitude. One signal channel is coupled to the vvm (input B). The remaining signal channel is not used in this test. A reference signal is introduced by the reference combiner circuit PDI using the same oscillator signal used in the beamforniers. A manually variable attenuator is present in the circuit to compensate for losses in the beamformer circuit. The power divider PD4 produces two reference signals (FREQUENCY REFERENCE and AMP/PHASE REFERENCE) of equal amplitude. The AMP/ PHASE REFERENCE signal is coupled to the vvm (input A) for comparison with the test signal from the frequency select matrix. The FREQ REFERENCE signal is not used in this test. The vvm measures the amplitude and phase relationship of the fundamental components of the AMP/PHASE REFERENCE signal and the AMP/PHASE TEST signal. A signal voltage proportional to amplitude and a signal voltage proportional to the phase differential is produced by the vvm. These two signal voltages are interpreted by a/d converters and routed to the cable scanner in the system control group. The output, in the form of a binary coded decimal signal is coupled through the signal data converter to the cable scanner in the system control group. The outputs of the test circuitry are analyzed by the computer. Any unacceptable condition is identified by a teletype output message.

e. Antenna Elements Testing. The antenna elements are tested by routing oscillator signals through the element test input matrix. The antenna element test matrix applies an oscillator signal to a selected antenna element through the directional coupler. A portion of the applied oscillator signal is reflected back along the input line and passes back through the directional coupler to the beamformers. The oscillator signal is then coupled through the antenna group beamformers to the beamformer output directional couplers. The system control group computer sets the beamformer test output matrix to select the appropriate antenna element beamformer. The oscillator signal is coupled to the vvm for amplitude measurements as previously described.

f. Switch Matrix Testing The switch matrix is tested in a manner similar to the beamformer. The olm&t test input matrix applies a selected oscillator signal t a selected input line and the reference combiner circuit. The FREQ REFERENCE d A, !P/PIHASE REFERENCE signals are produced in a manner identical to the beamformer test. FREQ REF signal is not used in this test. The oscillator signals coupled through the beamformers are routed through the directional couplers to the switch matrix. The computer in the system control group selects the matrix path to be used and tested. The output of the switch matrix is coupled to the operator position, if in use, and to the sampling matrix olm&t. The sampling matrix receives a switch closure signal from the group C digital interface unit (diu) DIU-C and a single output is routed to the band select matrix B4. Matrix B4 routes the signal to the appropriate group of bandpass filters. The bandpass filter rejects all frequencies other than the selected oscillator frequencies. The output of the filter is coupled through the frequency select matrix to the test circuit and the vvm. The vvm measures the amplitude of the fundamental component of the AMP/PHASE REF signal and the AMP/PHASE TEST signal. A binary word proportional to amplitude is produced and coupled to the system control group computer. An amplitude abnormality causes the computer to output a fault message on the teletype.

g. Oscillator Test. (See figure 7-5.) The oscillator test checks the frequency of each of the 18 oscillators that can be selected for olm&t functions. Referring to

figure 7-5, sheet 2, band B, observe that the reference output (oscillator reference output, band B) is output from matrix A1B and is connected to an input port of power combiner PDI. This signal progresses through the variable attenuator, power divider PD4, is selected as an input by the frequency counter input matrix 85, and is counted. The frequency count is then compared to that stored in computer memory and the test proceeds to the next oscillator until all have been tested.

4-4. Monitor Subgroup. (See figure 4-4.)

The monitor subgroup is housed in a low-profile cabinet. This cabinet is called the Console, Operation and Maintenance OJ-263/FLR-9(V) (somc). The somc contains three power supplies, a controller assembly, and a control panel. The controller assembly houses circuit cards that provide display and control circuitry for the somc control panel. The somc control panel provides a supervisory overview of system conditions at selected points as well as computer control. Four olm&t test request controls are also provided. Other nonautomatic tests can be requested via the tty terminal. The tty terminal also provides hard copy readout for test reports as well as equipment fault notifications. An explanation of the function of each of the controls and indicators is given in section III (Operation).

4-5. Power Distribution.

a. Olm&t Subgroup. (See figures 7-3 and 7-4.)

1. Ac power for the four olm&t racks is supplied by an external circuit breaker. Incoming power to rfi test rack 411 is filtered as a precaution against interference. The power supply in rack 414 supplies dc voltages to the group A and B matrix digital interface units. All other equipment in these racks that require a power source have self-contained power supplies.

2. Ac power for the group C matrix is obtained from the jack panel frame distribution. Dc voltages are supplied to the diu for the group C matrix by the power supply furnished for that purpose.

b. Monitor Subgroup. (See figure 7-2.) Ac and dc power distribution for the somc (217) is shown in the schematic diagram in section VII of this manual. Incoming power is controlled by a circuit breaker. Emi filtering is provided as the power enters the cabinet. The ac power is then split four ways to supply the cooling blower and three power supplies, through their fuses. Dc power in the form of +25 volts, +5 volts, and -7 volts is distributed to the various cabinet distribution points as shown in the schematic.

4-6. Olm&t Subgroup Detailed Description.

a. Principles of Operation. (See figure 7-5.) The monitor and test group per-forms diagnostic test routines to monitor the performance of the following beamformers:

48 monitor beamformers in band A
48 monitor beamformers in band B
24 monitor beamformers in band C
3 omni beamformers (one in each band)
9 sector beamformers (three in each band).

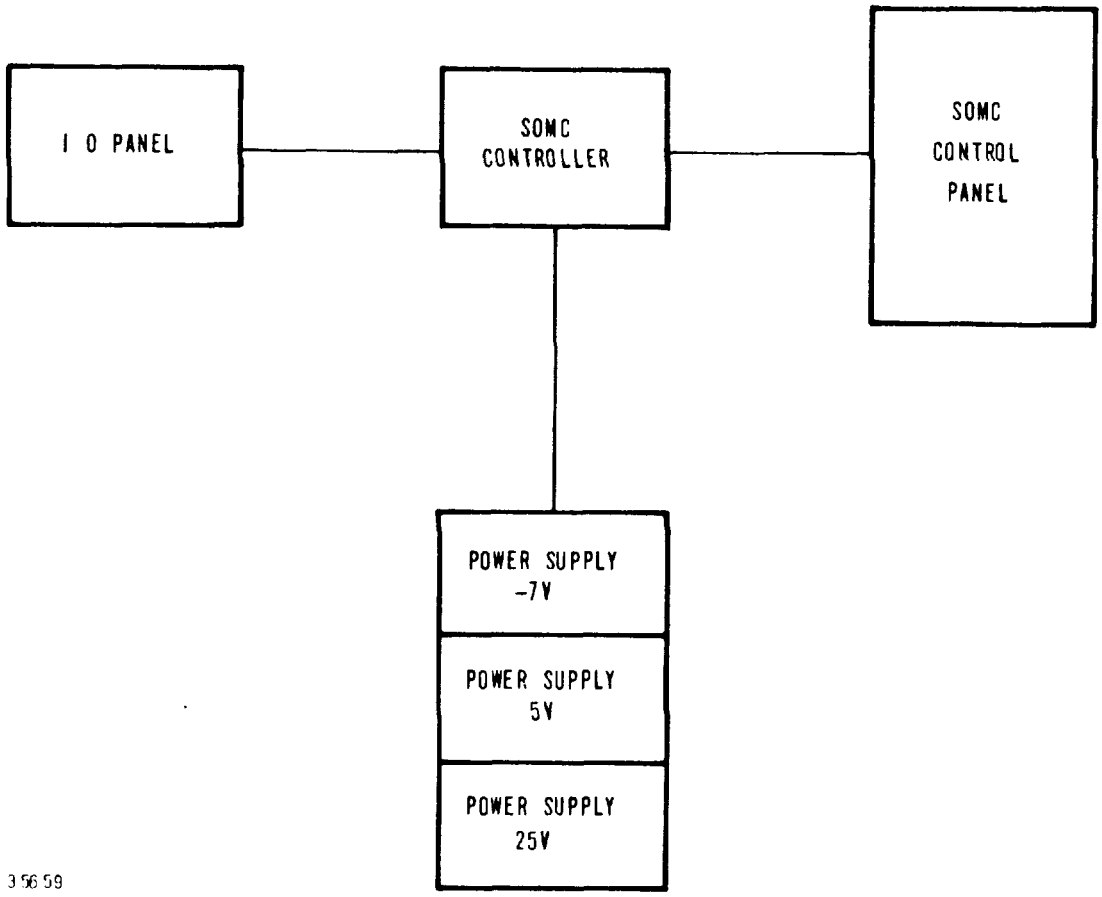


Figure 4-4. Simplified Block Diagram, Somc

Diagnostic test routines also monitor 48 band A antenna elements, 96 band B antenna elements, and 48 band C antenna elements. The diagnostic test routines also may analyze 42,080 crosspoints to completely check out the operation of the switch matrix group. The beamformers and antenna elements contained in the AN/FLR-9(V7) and (V8) sites are depicted as a single unit for bands A, B, and C in figure 7-5. The operation of the olm&t circuit is identical in each band and in each antenna element within each band.

1. Test Signal Oscillators. (See figure 7-5.) Six test signal oscillators are provided for each of the three bands. Each oscillator is a ruggedized, solid-state, sealed plug-in unit. The frequency of each is listed in table 4-4. For stability, these oscillators are crystal controlled, air cooled, power source regulated, isolated, and operated continuously.

Table 4-4. Test Oscillator Frequency

Band	Oscillator	Frequency (in MHz)
A	1	1.5
	2	2.0
	3	3.0
	4	3.5
	5	4.5
	6	6.0
B	7	6.0
	8	7.5
	9	9.0
	10	12.0
	11	14.0
	12	18.0
C	13	18.0
	14	19.0
	15	22.0
	16	24.0
	17	27.0
	18	30.0

2. Variable Attenuators. (See figure 7-5.) One attenuator is provided for each signal source oscillator in each band and a variable attenuator is also used in the input network to the vvm. The oscillator attenuators are mounted on a front panel section, one panel for each band. Each attenuator is adjustable from O dB to 10 dB. Each is adjusted to a standard output level. Specifications for these attenuators are given in table 1-2 and adjustment is explained in section V, paragraph 5-13.e., phase and amplitude adjustments.

3. Select Matrix Group A. (See figure 7-5.) Test oscillator output connection is accomplished by group Al matrix switching. The oscillator select matrix

Al is a computer-controlled reed switch matrix that provides load isolation for the test signal oscillators and prevents oscillator signal leakage to the system. The switch is designed so that each oscillator is terminated with the proper resistive output impedance. Matrix control is provided by the diu for group A.

4. Test Signal Bandpass Filters. (See figure 7-5.) Bandpass filters are necessary to exclude all signals within the bandpass of the vvm except the test signal. The filters selected are narrowband (see table 1-2) crystal bandpass filters. Any signal that is slightly off-center is attenuated. At 0.1 percent from the center frequency, the attenuation is 60 dB. The very sharp response curve skirts aid the vvm in acquiring the test signal.

5. Select Matrix Group B. (See figure 7-5.) The group B matrix provides signal switching in the test circuits for selection of the proper filter for each band as well as the filter input signal. Another portion of the group B matrices alternately connects a sampling of the oscillator reference signal and the signal under test to the frequency counter. Control of signal routing is by the decoding of signals in the diu from the matrix multiplexer in the system control equipment group.

6. Sampling Matrix Group C. (See figure 7-5.) The olm&t sampling matrix : elects one of the 800 outputs (for V8) or the 400 outputs (for V7) from the switch matrix. In addition, at the V8 site one of five inputs may be selected from the special project matrix. Part of group B matrix then selects the test circuit for the desired filters, and applies the test signal to the group B test output matrix servicing that band. Control for the group C matrix is provided by the group C diu, which decodes instructions from the matrix multiplexer.

7. Directional Couplers. (See figure 7-5.) The output of the group A test : select matrix is fed into the antenna system or beamformer network through directional couplers. After the test signal has been routed through the antenna elements and/or the beamformer networks, the signal is either sampled from a beamformer output directional coupler or routed onward into the switching matrix. The input couplers have two signal insertion ports. One is used for antenna element test and the other is directed to the beamformer network input. The beamformer output couplers have one output sampling port for olm&t test purposes. All ports of these directional couplers are constantly terminated in 75 ohms to prevent impedance mismatching.

8. Power Combiners and Dividers. (See figure 7-5.) Two power combiners are used in the input of the olm&t metering circuits (PD1 and PD2). Each of these combiners has a common output for any one of the three inputs. Since only one band is tested at a time, only one reference signal at a time is presented to an input port a, the PDI and PD2 combiners. Each input port is isolated from the others. All ports .re terminated in 75 ohms at all times. The two power dividers (PD3 and PD4) are used to split reference signals between the two metering circuits. One input is divided into two outputs. Output ports are isolated from each other and all are , matched at 75 ohms. Specifications for the power combiners and dividers are given in section 1, paragraph 1-5, Capabilities and Limitations.

9. Frequency Counter. (See figure 7-5.) The frequency counter input is determined by the state of the group B input select matrix. An input is selected, either from the olm&t filter circuit under test, or from the oscillator reference output being used. The frequency counter outputs eight digits of information using 4-2-2-1 binary code to express digits from 0 to 9. These 32 signal outputs are routed to the signal data converter for signal conditioning. The eight output digits are interpreted by the computer for comparison to a reference reading stored in memory. Specifications for the frequency counter are given in section 1, paragraph 1-5, Capabilities and Limitations and in the manufacturer's equipment handbook, Specification H33-5245M, commercial manual CM 32-6625-239-14.

10. Signal Data Converter. (See figure 7-5.) The signal data converter provides part of the olm&t test circuit interface from the vvm and frequency counter to the cable scan multiplexer in the system control group. The signal data converter is a signal conditioner that handles three signal groups. These are the vvm control signals, the VVM PHASE UNLOCK signal, and the binary coded decimal (bcd) output of the frequency counter.

(a) Vector Voltmeter Control Signal Group. (See modification sheets for H168405A vvm manual and figure 7-6.) The vector voltmeter (vvm) control group remotely selects test ranges in the voltmeter by activating relays inside the vvm. Control signals are for vvm amplitude range, phase range, frequency range, 180-degree offset, and channel select. Amplitude ranges are selected in nine steps by individually grounding pins 17 through 25 of JO11 on the vvm. The amplitude range control action is initiated by four control lines from the system control group to the signal data converter. These lines are held at voltage levels to the differential receivers and introduced to a decoder. The decoder decodes the four input signals to nine control signals, one for each of the nine amplitude ranges. The nine control signals are fed to nine voltage translators which ground the appropriate line to select the desired amplitude range. Phase ranges are selected in four steps by no pins grounded or pin 14, 15, or 16 of JlO1 ungrounded. Phase ranges are 6, 18, or 180 degrees. The phase range control action is the same as that for amplitude control except that action is indicated by two control lines at J5 which are decoded to three control line outputs at J2. Frequency ranges are selected in five steps by individually grounding pins 1 through 5 of J101 on the vvm. Frequency ranges are 1 to 4 MHz, 4 to 7 MHz, 7 to 12 MHz, 12 to 30 MHz, and 30 to 60 MHz. The frequency range control action is initiated by three input lines decoded to five outputs at J2. The 180degree phase offset is used for weak signals greater than ±50 degrees and improves the angle resolution. Pin 27 of J101 is grounded for operation between ±150 degrees. Beyond +150 degrees, pin 27 is ungrounded and the meter is offset for greater resolution. The channel selection function is used to select either channel A or B as the vvm input. Grounding pin 13 of JO11 selects channel A and not grounding it selects channel B. The 180-degree meter offset action is initiated by an input line from the system control group at J5. This signal is strobed through the logic, is amplified, and is conditioned by the voltage translator to ground or raise a control line at J2. The channel select action is identical to the 180-degree meter offset and grounds or raises one output line from J2 on the signal data converter.

(b) Frequency Meter Output Drivers. (See figure 4-5.) The frequency meter output is a four-place binary coded decimal (bcd) of eight digits using a 4-2-2-1 code to express digits from 0 to 9. One of the eight digital groups is shown in the block diagram. The four bcd inputs at Jl (for each digit) are strobed into the logic and line drivers. Each bcd input has a line output. There are 32 output lines for the 32 bcd inputs. The data lines are scanned periodically by the cable scan multiplexer of the system control group.

(c) Vvm Phase Unlock Indication. (See figure 4-5.) The vvm phase unlock indication is an informational feedback to show whether or not the vvm automatic phase control (apc) is tuned to the incoming signal. An unlocked indication shows that the amplitude and/or phase ranges are not properly set and calls for range changes from the computer. The vvm apc unlock is a single line from JO11 of the vvm to J2 of the signal data converter. This line is conditioned by a logic and line driver stage and is output on a single line at J5 to the computer.

(d) Power Supply, 3300-44037. (See figure 4-6.) In the signal data converter power supply, the 120-volt ac input is reduced by a step-down transformer. The stepped down ac voltage is rectified and filtered by two separate circuits. The load rectifier and filter supplies 5 ±0.5 volts dc at 4 ±0.4 amperes to the series regulator. The internal rectifier and filter supplies 5 ±0.5 volts dc to bias the internal reference zener diode and to provide power for the internal driver and control transistors. The internal rectifier and filter supplies dc voltage and current to the series regulator which is connected in series with the output. The voltage across the series regulator varies as the input voltage, load, and other conditions change to maintain a set output voltage. The series regulator is controlled by the regulator control circuit error voltage. The error voltage is generated by the regulator control circuit which compares two inputs, a reference voltage from a zener diode and the output voltage. The difference between these two voltages is sensed and an error signal is produced. The error signal is amplified and used to control the voltage across the series regulator. The over voltage circuit samples the output voltage of the series regulator. When this voltage exceeds a preset value (+6 volts dc) the overload circuit is saturated. As a result, the regulator control circuit and the series regulator are cut off to cause the output voltage to decrease. The over voltage circuit is an SCR crowbar type. In the circuit a reference voltage is compared to the output voltage. The resultant error voltage drives the SCR into conduction when a preset value is obtained. The SCR, while conducting, shorts (crowbars) the output.

11. Vector Voltmeter (vvm). (See figure 7-5.) The vvm is provided to read the voltage of either input A or input B and the phase difference between the two signals. In this way, the test oscillator reference voltage is compared directly with the signal from the circuit being tested. The vvm is remotely controlled by the computer matrix multiplexer through the signal data converter. Specifications for the vvm are given in section 1, paragraph 1-5. Complete technical information is provided in the manufacturer's equipment manual, Specification H16-8405A, commercial manual number CM 32-6625-240-14.

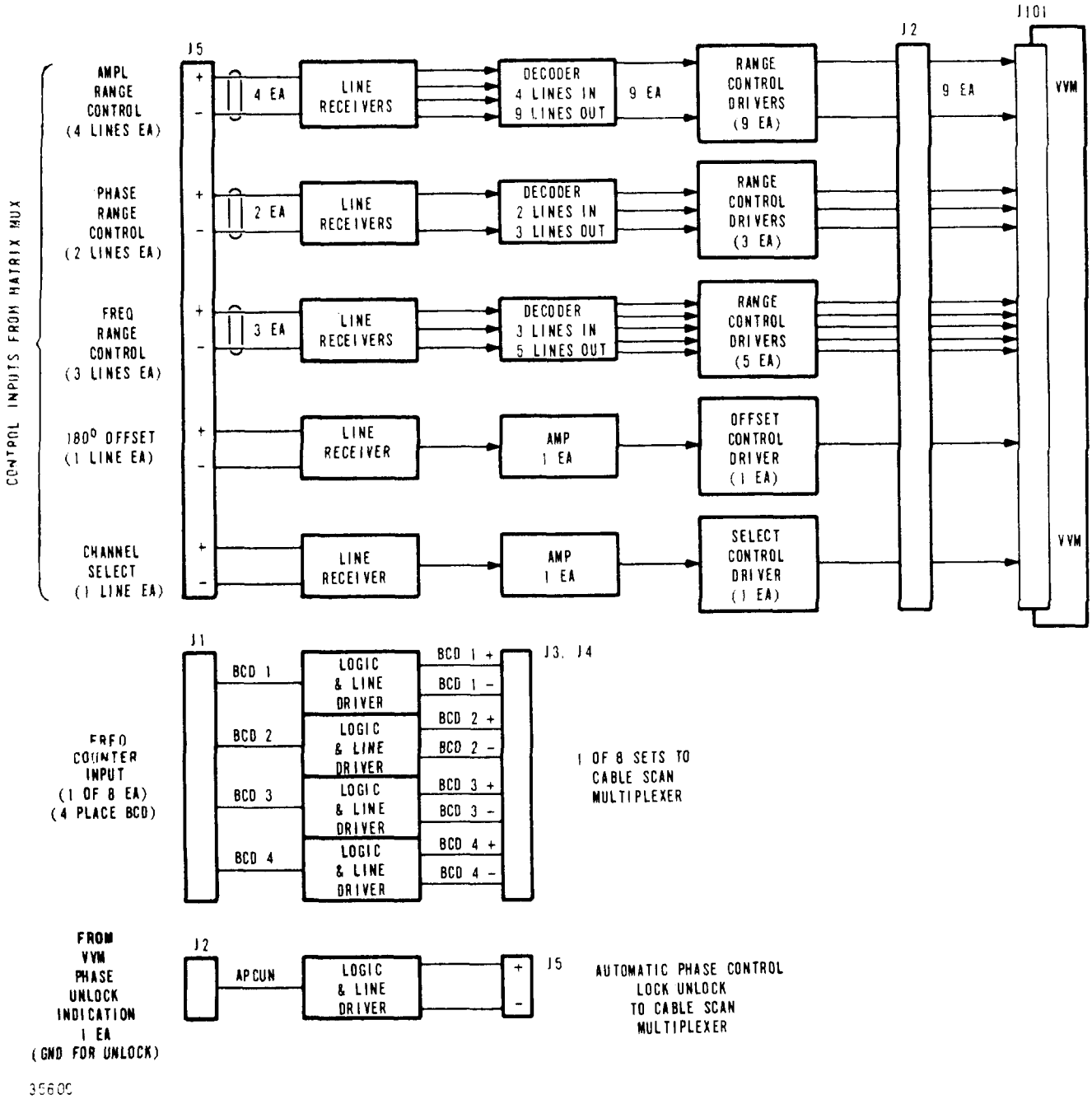


Figure 4-5. Simplified Block Diagram, Signal Data Converter

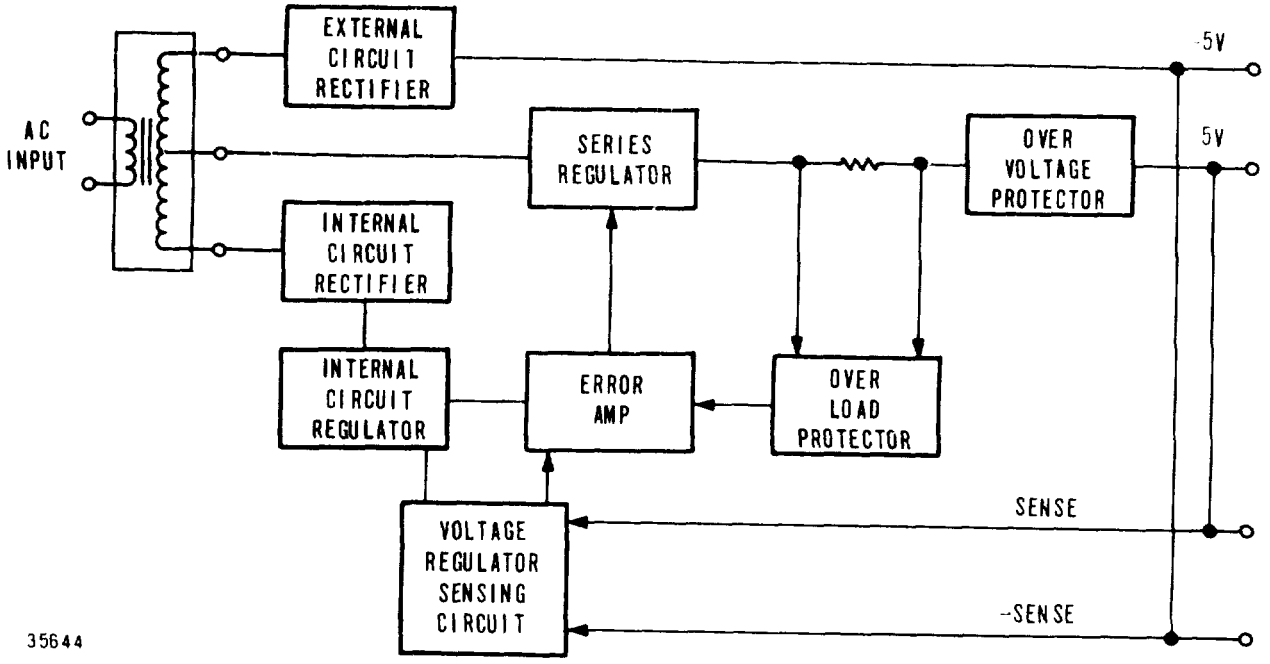


Figure 4-6. Power Supply, Signal Data Converter

12. A/d Converters. (See figure 7-5.) Two a/d converters are provided to convert the analog voltage and phase outputs of the vvm to binary digit code. These converters are controlled by the matrix multiplexer. The converter outputs are fed to the cable scan multiplexer. Specifications for the converters are given in section 1, paragraph 1-5. Detailed description of the equipment is given in the manufacturer's equipment manual for Part No. 52100 and 52100-1, commercial manual CM 325820-241-14.

13. Test Routing. (Based on figure 7-5, see figures 4-7 through 4-10.) Routing of the various olm&t tests is shown in the block diagrams, figures 4-7 through 4-10. An overall picture of test routing can be seen by following the route of each band on figure 7-5, the intercept group olm&t block diagram.

b. Electronic Circuits.

1. Signal Data Converter. (See figure 7-6, sheets 1 and 2.) An input signal of each type is traced through the signal data converter logic diagram to familiarize personnel with the functional logic. Board schematics are found in section VII (Maintenance Illustrations). Consult paragraph 7-2 for logic explanation.

(a) Control Signal Group. (See figure 7-6, sheet 1, upper left corner.) Observe that pins AB, ED, GH, and LK of J5 are amplitude range control input numbers 1, 2, 3, and 4. Referring to the logic diagram for 9615 located at the right side of

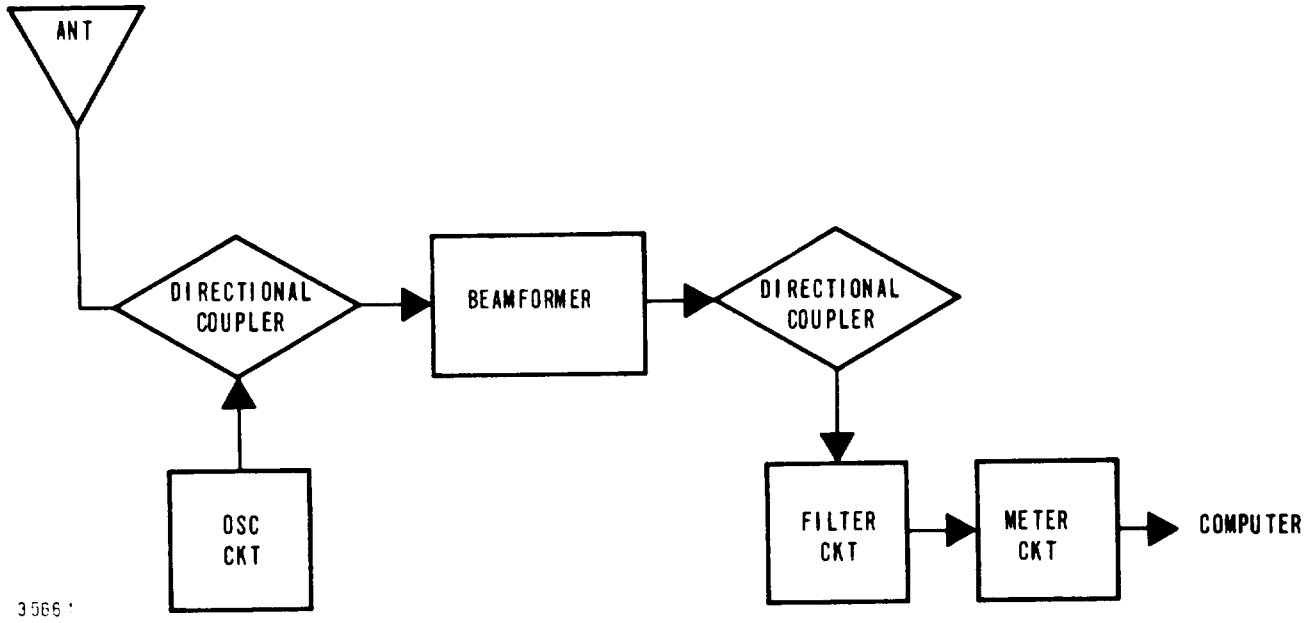


Figure 4-7. Routing Diagram, Beamformer Test

the page, observe that pin A of J5 is the +INA input at pin 5 of the logic unit 1H7A. Observe that pin B of J5 is the corresponding negative input to pins 6 and 7 of the logic unit. Pins I and 2 of the logic unit are the AMP I-P output. Observe that pins D and E of J5 are connected in like manner to output AMP 2-P at pins 14 and 15 of the logic unit. AMP 3-P and AMP 4-P are developed in the same way. Observe that AMP 1, 2, 3, and 4 are connected to a decoding network so that different combinations of these signals raise one of the nine outputs at a time. Note, for example, that the D-70 DB-P output is raised by AMP 1 going positive and AMP 2, 3, and 4 going negative. AMP 2, 3, and 4 are inverted, in this case, making all four inputs to the IG4B decoder NAND gate positive and lowering its output. The output is inverted and amplified by IF4B giving a positive D-70 dB output. Observe that the D-60 dB output is made positive by AMP 2 going positive with AMP 1, AMP 3, and AMP 4 going negative, making four positive inputs on IG4A NAND gate. The IG4A output is inverted and amplified by IF4A to produce a positive D-60 dB output. Each of the nine outputs are decoded in this manner. Turning to sheet 2 of figure 7-5, upper left portion, locate the D-70 dB input to Q1. Note that this input is pin 28 of the circuit board and that all of the control signals input to this driver board. Q1 and Q2 form a driver that presents a low to the selected pin of the vvm to activate a control relay. Q1 through Q18 are the drivers for the vvm control functions. Note that the driver outputs connect to pins 17 through 25, and pin 11, of J2. J2 connects to the corresponding pin numbers of J1O1 on the vvm. Referring again to figure 7-5, sheet 1, left side, note that J5, pins N and P are PHASE plus and minus. These are converted to signals

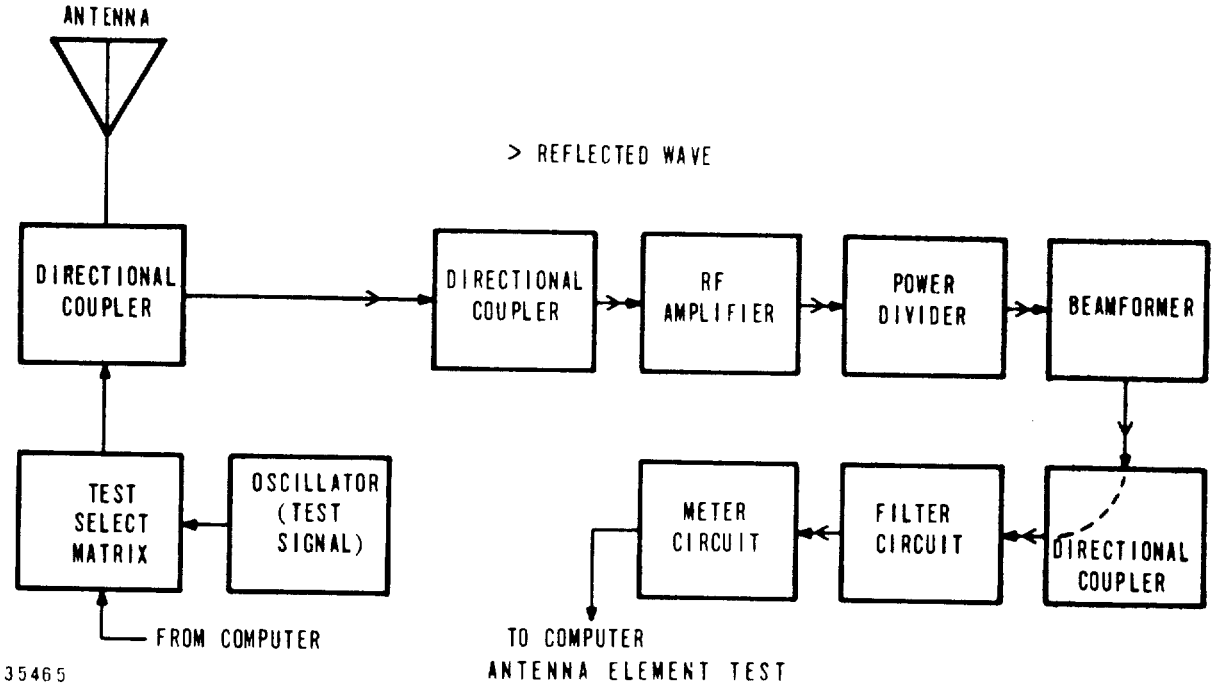


Figure 4-8. Routing Diagram, Antenna Element Test

PHASE I-P and PHASE 2-P by logic block 1F7A. These two signals are binary code for the four phase range control signals. The binary inputs are decoded by inverteramplifiers ID4A and 1D4B, NAND gates IC4A, B, and C, and inverter-amplifiers IC4D, E, and F. There are four decoded conditions with binary 000 being the 6-degree range, 001 is the 18-degree range, 010 is the 60-degree range, and 100 is the 180-degree range. Three lines are used to control the four phase ranges. Refer to figure 7-5, sheet 2, left side. The three phase range control lines are input to the bases of Q1, Q3, and Q5 of the lower circuit board. These three control drivers are identical in action to those described for the amplitude control drivers. Referring to figure 7-5, sheet 1, left side, note that the FREIN 1-P, 2-P, and 3-P signals, plus and

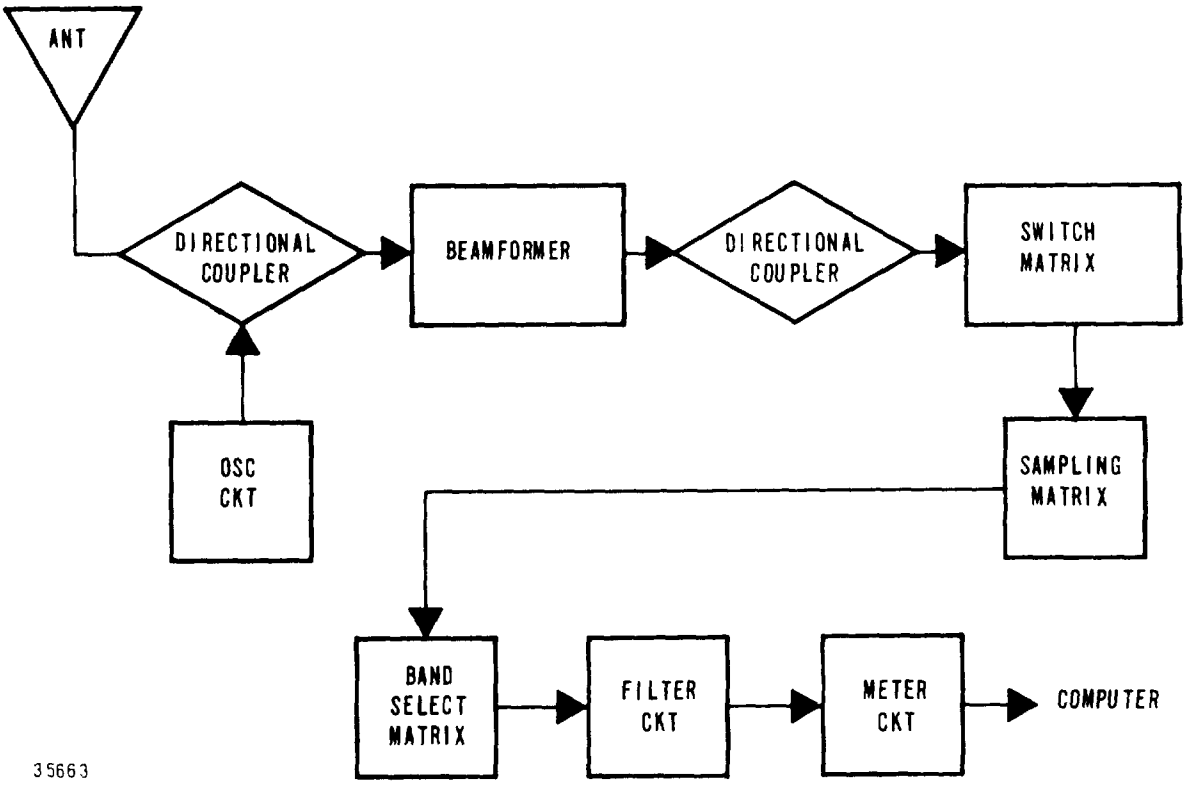


Figure 4-9. Routing Diagram, Path Verification Tests

minus, are formed into the FREQ 1-P, 2-P, and 3-P binary code signals. These signals are processed by the decode circuitry to produce the five frequency range signals that are fed to the vvm through the control drivers. OFFSET-P plus and minus is converted by logic to the 180-degree OFF-P signal that is routed through two inverteramplifiers and the control drivers shown on sheet 2. SELECT-P plus and minus is converted to the CHANNEL-P signal and is processed and routed to the vvm to select either A or B channel input.

(b) Apc Unlock Signal. (See figure 7-6, sheet 2, upper left corner.) The apc unlock signal (APCUN-P) notifies the computer that the vvm is not set to the proper amplitude and/or phase range for the incoming signal. Locate the pin 11 of J2 that is adjacent to the O-dB driver output at pin 25. Note that this is labeled APCUN-P and that this pin receives positive supply voltage through isolation resistor R31. At bottom center of the drawing field, locate logic block 2B4B and its input which is also APCUN-P. This input at J2, pin 11, Is the same point as the APCUN-P receiving supply voltage. J2 pins 11 and 12 are connected to J101 pins 11 and 12 of the vvm. These pins connect to contacts inside the vvm that are closed during a phase unlock condition. Therefore, the input to line driver 2B4B is held at positive supply voltage unless a phase unlock occurs, which grounds the input (connects pins 11 and 12). The 2B4B line driver is connected to J5 which is connected to the matrix controller of the system control group.

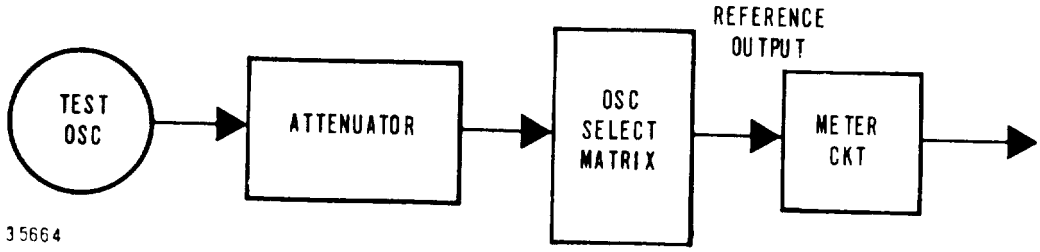


Figure 4-10. Routing Diagram, Oscillator Test

(c) Frequency Counter Output Group. (See figure 7-6, sheet 2.) The output of the frequency counter is a 32-bit bcd number. Each digit is coded from 0 to 9. There are 32 bcd inputs to the counter output line drivers located in the signal data converter. Bcd input is through J1 pins 1 through 16 and pins 26 through 41. The bcd inputs are ±5 volts dc for a "1" and O volt dc for a "O". Each bcd input is ANDed into the logic where it is amplified and converted to a dual polarity line signal by a line driver. (Refer to figure 7-6, logic diagram 9614 at the right of the drawing.) These signal output lines are divided into a low order output word from J2 and a high order output word from J1 (see figures 9-5 and 9-6). The two output words are routed to the cable scan multiplexer in the system control group.

2. Power Supply, 3300-44037. (See figure 7-7.)

(a) Rectifier. The 110-volt ac input voltage is stepped down by transformer Tl. The stepped-down voltage is applied to rectifiers CR1, CR2, CR3, and CR4. Rectifiers CR1 and CR2 form a full-wave rectifier which supplies current to the external load through series regulator Q8. Rectifiers CR1, CR2, CR3, and CR4 form a bridgetype rectifier which supplies current to internal circuits. The external supply (CR1 and CR2) is filtered by capacitors C1 and C2. The internal supply is filtered by C6.

(b) Series Regulator. The negative dc line is coupled directly to the negative output. The positive dc is connected through the series regulator transistor Q8 and emitter resistors R18 and R21 to the positive output. Control of Q8 results in regulator action against line and load changes.

(c) Voltage Regulator. A sample of the output voltage from R15 and R16 is compared by the differential amplifier Q3 and Q4 with a reference voltage derived from a zener reference element and divider R2 and R3. When Q4 conducts, the base drive is reduced to Q6, Q7, and Q8. Controlling the base drive of Q8 provides regulator action.

(d) Internal Circuit Regulator. CR5, a zener diode, is the reference voltage for two open loop constant current sources QI, R4, and Q2 with R8. Q1 and R4, maintain a constant bias current through the reference element CR6 and divider R2 and R3. Q2 and R8 provide constant current for Q4 and driver transistor Q6.

(e) Overload Protection. The load current is sensed by the voltage drop across R18 and R21. The overload circuit conducts and reduces the base current of Q6 which provides current limiting. At short circuit, the loss of output voltage and the bias level set by divider R13 and R14 cause the short circuit current to be limited to a value less than rated current.

(f) Overvoltage Protection. Overvoltage protection is provided by the overvoltage assembly. This protection is accomplished through the high current capacity of CR5. CR5 conduction is controlled by an error signal generated by differential amplifier consisting of Q1 and Q2. The error signal is generated by comparing the load voltage to a reference voltage produced by CR1. When the load voltage rises by more than 2 volts (adjustable by R7), the error signal drives Q3 into saturation. The saturation current of Q3 drives CR5 into conduction. While conducting, CR5 places a very low impedance across the power supply output, thus reducing the load voltage.

3. Olm&t Power Dividers and Combiners. (See figure 7-5.) Power dividers and combiners are used in the olm&t subgroup as shown in the referenced figure. Power dividers in the olm&t subgroup provide a minimum of 30-dB isolation between ports.

(a) Two-Output Power Divider. (See figure 7-9.) This power divider has one input port, J1, and two output ports, J2 and J3. Transformer T1 is an impedance matching transformer that matches the 75-ohm input impedance to the output splitter transformer T2. T2 splits the signal into two equal parts for output to J2 and J3. Windings 1-1' and 2-2' are bifilar wound. The two windings are connected so that mutual inductance is aiding when a signal is applied as shown. Capacitor C1 helps maintain broadband operation as well as improving vswr. Resistor R1 is provided to present a 75-ohm output impedance on each port, maintaining a low vswr.

(b) Three-Input Power Combiner. (See figure 7-10.) This power combiner hat one output, J1, and three inputs J2, J3, and J4. J2 and J3 are inputted to splitter windings 1-1' and 2-2' mutually aiding each other to overcome losses. Resistor R2 matches impedances at each input. The output of T4 (pin 3) connects to pin 1 of T2. The J4 input is connected to pins 1 and 2' of T3. T3 is connected to benefit from the mutual inductance of the two bifilar windings and provide impedance matching to 75 ohms and to the transformer T2. Transformer T2 is an impedance matching power divider that balances inputs J2, J3, and J4 to its output at pin 4. R1 is connected between the two inputs and across T2 to maintain broadband response and aid in impedance matching. C1 helps maintain broadband operation and impedance matching. Transformer T1 functions as an output step-up transformer that matches impedance to output port JI and compensates for circuit losses.

4-7. Monitor Subgroup Detailed Description.

a. Principles of Operation. The monitor subgroup hardware occupies portions of the somc (unit 217). The nearby teletype units are computer controlled and functionally integrated with the somc control panel for overall control and supervision, of the system. The operating procedure for this position is included in paragraphs 3-3 through 3-7. Each control and/or indicator of the somc control panel is located and explained in paragraph 3-2 of section III. Items located on the somc control panel are classified as alarms, status indicators, controls, and panel functions. Each item has its own functionally separate operating circuit. For convenience in the explanation of operating principles, these circuits are grouped as input, output, and panel functions.

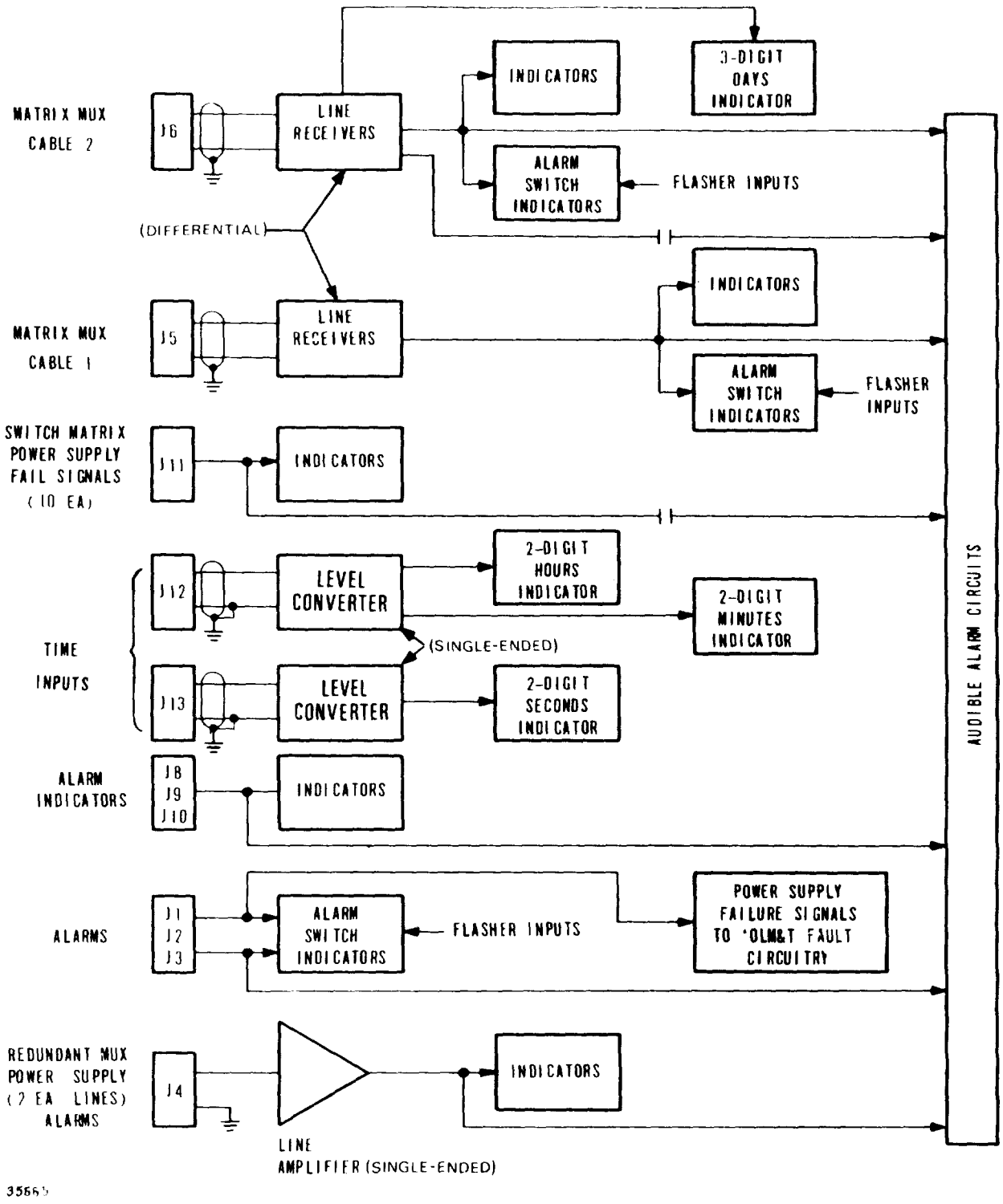


Figure 4-11. Simplified Block Diagram, Somc Input Circuits

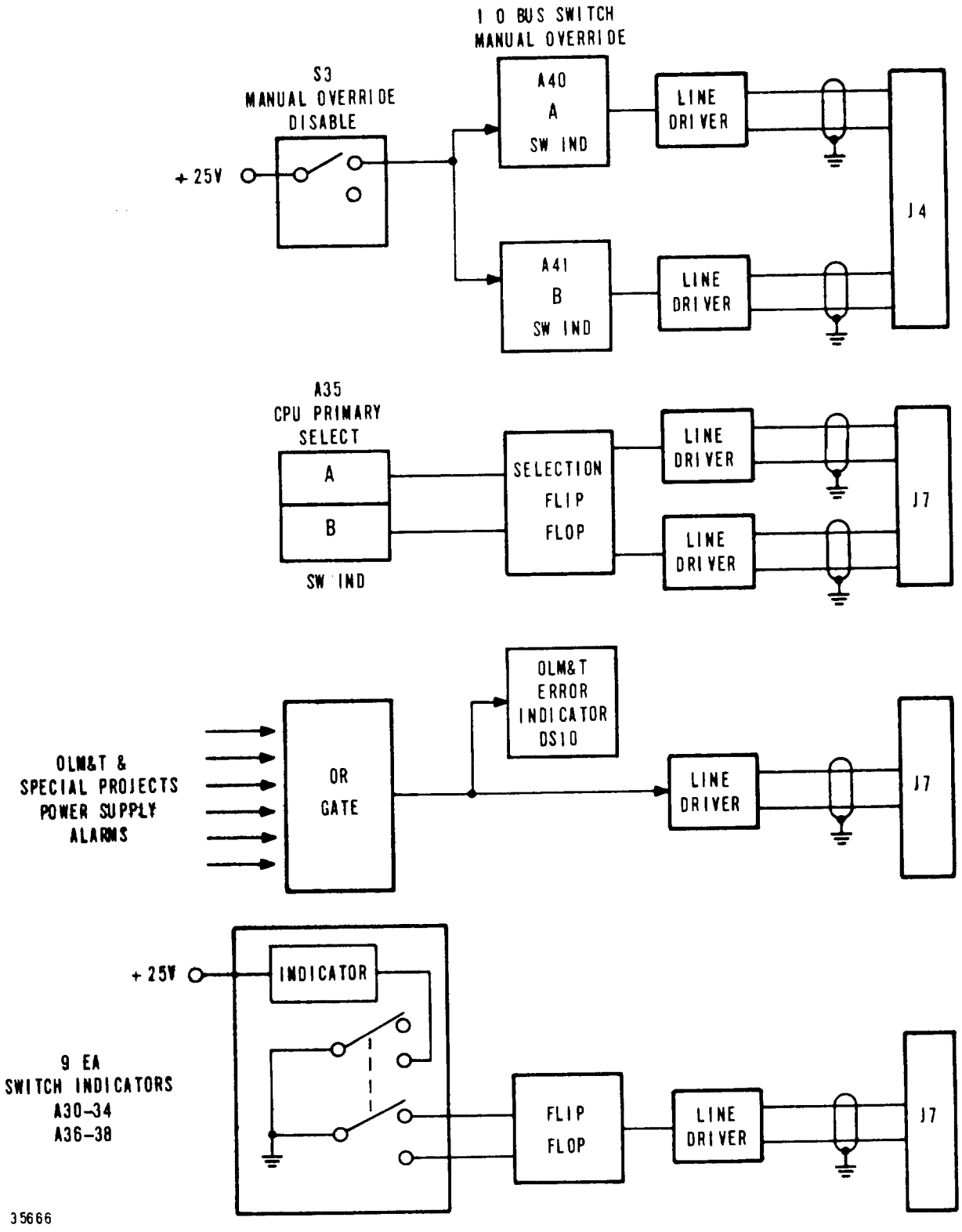


Figure 4-12. Simplified Block Diagram, Somc Output Circuits

1. Input Functions. (See figure 4-11.) Somc input circuitry types are shown in the simplified diagram in figure 4-11. Inputs are generated by either computer or hardware situations being monitored. Hardware alarms are airflow, temperature, and power failures. The computer input reports of the status of malfunctioning of the magnetic tape units, tty units, and the cpu. Status indications are provided by illuminating the indicator affected, and alarms are given by flashing red indicator and an audible alarm.

2. Output Functions. (See figure 4-12.) Somc output circuit types are shown in the referenced figure. These circuits set output lines that are either control requests or are giving status information to the cpu.

3. Panel Functions. (See figures 4-13 and 4-14.) Circuits performing a control panel function are the audible alarm circuit, the lamp test circuit, and the flasher unit, the output of which is routed to all alarm indicators.

b. Electronic Circuits. (Reference figure 7-8.) An explanation of somc circuitry can best be given by following a circuit of each type through the console logic diagram (figure 7-8) located in section VII. A simplified block diagram of each type of circuit has been described in paragraph 4-7.a. and the same sequence is used for this more detailed explanation. Reference to physical location on drawing sheets is made in vertical coordinates using letters and in horizontal coordinates using numbers as explained in paragraph 7-2 of section VII.

1. Input Circuits.

(a) Transmission Line Inputs. (Refer to figure 7-8, sheet 6.) Locate area D8 of the drawing referenced. At J5, pins w and v, the PRIMARY A indication is input from the computer matrix multiplexer. This is applied to pins 42 and 41 of the integrated circuit card the components of which function as unipolar line receivers. This integrated circuit is assigned the reference designator 6D7A which is also its location on the drawing sheet (sheet 6, location D7). The U3A designation specifies which of the identical circuits on the circuit board is being used. The A217 designation is the location of the circuit board upon which the integrated circuit is mounted (row A2, socket 17 of the somc controller card cage). Pin 43 of this card is labeled VCC. This notation means that this point is connected to a +5-volt bus. Circuit card pins 14 and 44 are the output of the line receiver and are connected to pin 12 of the card located at A218, circuit U3A. This circuit (6D6A) is a NOR gate controlling a transistor driver for the PRIMARY A indicator lamp (6D5A). When the input of 6D6A (pin 12) goes low, its output goes high (+5 volts), this turns on the lamp driver transistor which supplies ground to the indicator lamp circuit. Note that pin 13, output of 6D6A, is also connected to 6D6B, A211, capacitor C9. This capacitor is a transient suppressor and is used in all of the circuits with this application. Also connected to the output pin is a line output labeled lOF5A-57. This coding indicates that the wire is connected to a circuit on sheet 10 of this drawing, area F5, pin 57 of the diode board. This connection is to the lamp test circuit through a blocking diode. Note that all lamps are connected to the lamp test network shown on sheet 10. The long transmission line alarm inputs are input through line receivers and amplifiers also, except that there is a pulse forming network included to prevent erroneous alarm responses from pulse transients. Examples of these pulse forming networks are shown on sheet 9 of the drawing in areas F6, F7, and F8. On sheet 9, area F7, note that the pulse-forming network outputs are applied to NOR and NAND gating so that an alarm pulse, formed by

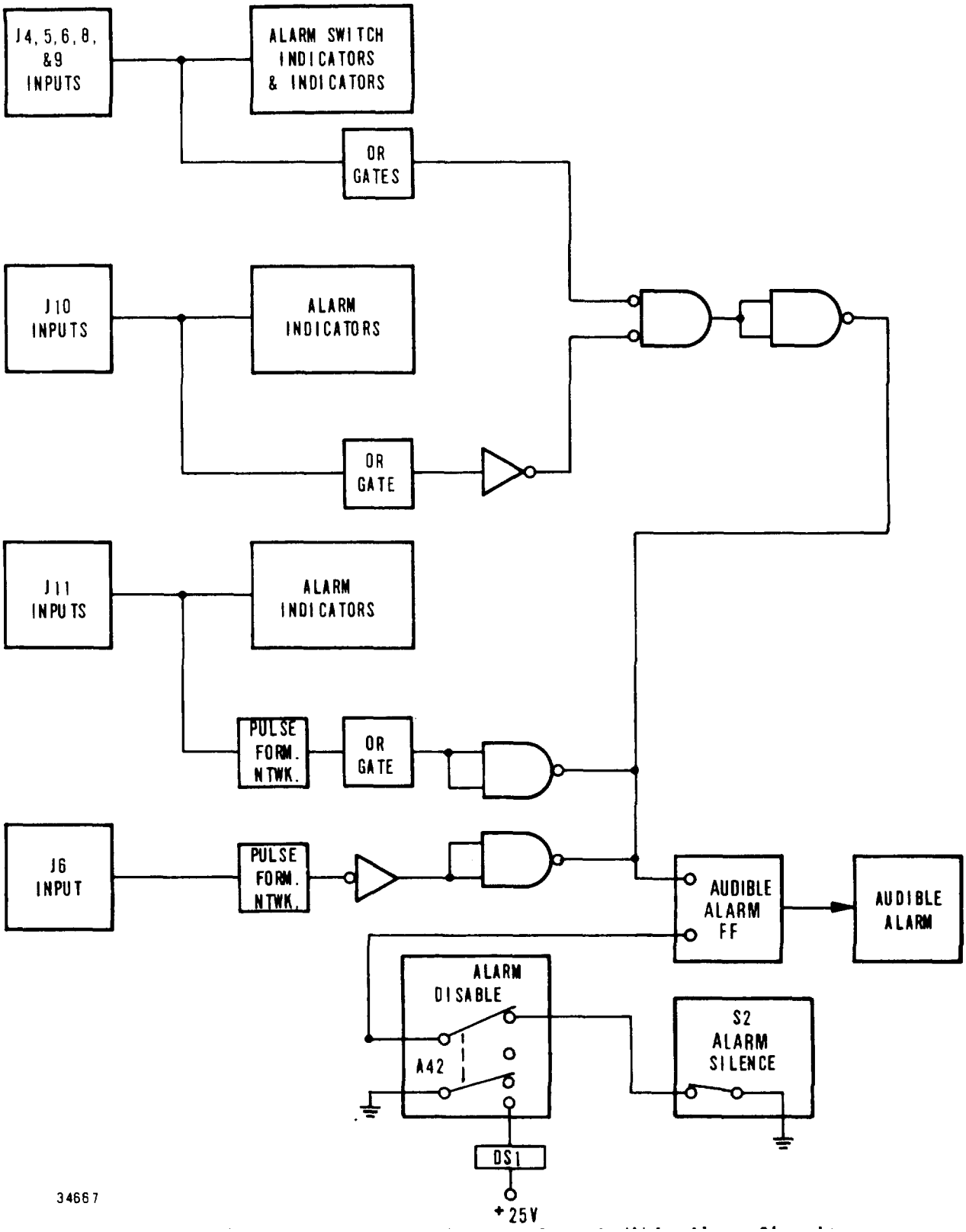


Figure 4-13. Simplified Diagram, Somc Audible Alarm Circuit

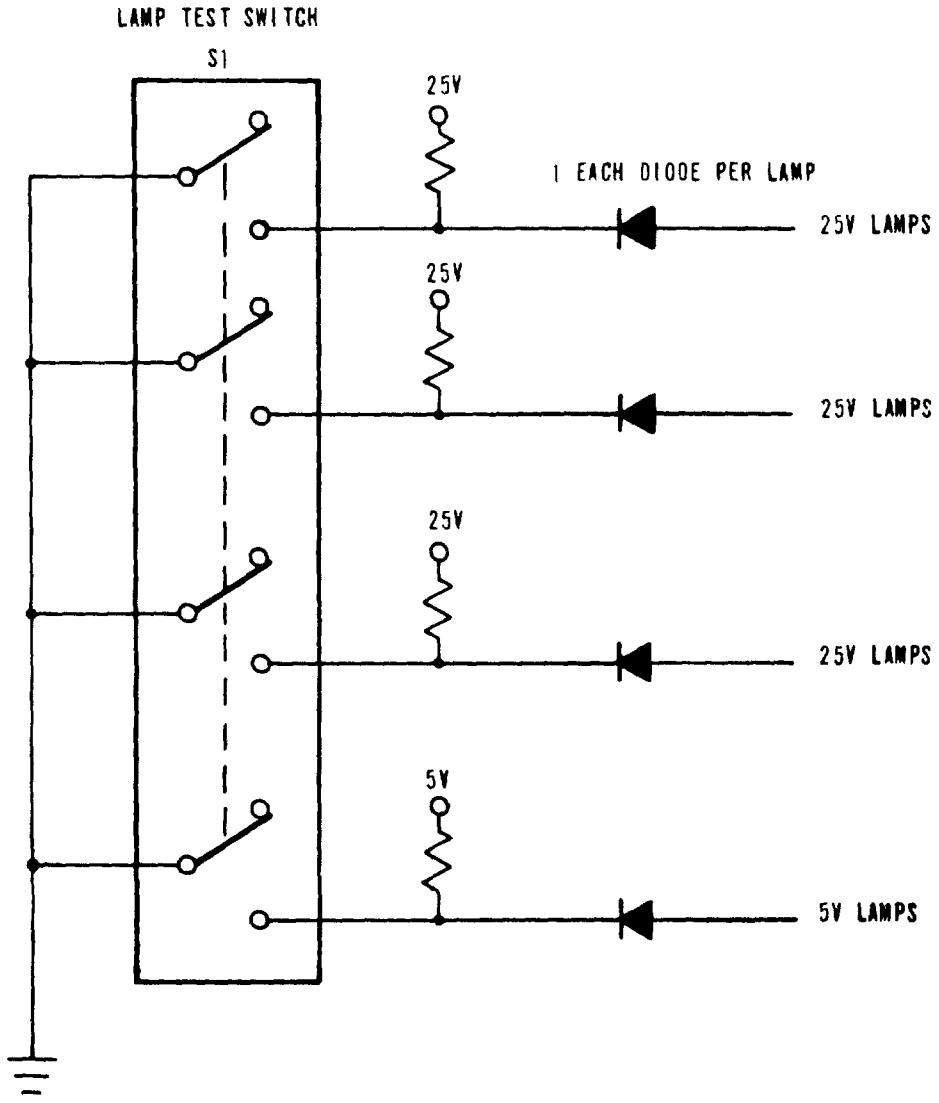


Figure 4-14. Simplified Diagram, Somc Lamp Test Circuit

a switch closure, causes the alarm latching flip-flop (9E6C and 9D6B) to set, turning on the audible alarm (DS74 9C5A).

(b) Local Alarm Inputs. (Reference figure 7-8.) An example of a local, wire input, alarm indicator is DS29, a switch matrix temperature indicator. The input to this circuit is shown on sheet 7 of the referenced drawing at area G8, terminal J8, pin G. These alarm circuits are external switch closures to ground. Therefore, DS29 is supplied with ground and is illuminated until the ground is removed. Also grounded is the line to 10C5A-46. Refer to sheet 10, area C3, pin 46 and observe that this is a connection to the lamp test circuit and a tie point leading to 8C7A-9. Refer to sheet 8, area C7, pin 9, and note that this is a connection to a capacitor board at row Al, socket 11 of the same controller. This blocking capacitor (C9) forms part of a pulse-forming network with R9 and CR9 at board location A110. Trace the circuit to area C6. Note that it connects to pin 28 of board location A113, an extended NOR gate as shown in area G5 (circuit U1). When pin 28 drops low, the output of 8C6E (pin 25) goes high. This signal high is connected to the inverting amplifier 8C5A, pin 18, and is output on pin 48 of board location A106. This output is routed to another extended NOR gate 8D2A, another inverting amplifier 8DIA, and becomes one of two inputs to the NOR gate 8D1B. Note that these gates are collection points for alarm signals.

(c) Console Clock Inputs. (Reference figure 7-8 and 5-19.) The days/hours/ minutes/seconds indicators mounted on the some front panel are controlled by two separate sources. The three indicators displaying the day number of the year are controlled by the computer. The six time-of-day indicators are controlled by the station master clock. The nine display units are identical. Each is capable of decoding four bcd inputs into the seven display elements necessary to display the numbers 0 through 9. By varying the number of bcd inputs and the base connections on the display units, all of the display requirements are fulfilled.

(1) Days Display Input Circuits. (See figure 7-8, sheet 4.) Days indicator inputs enter on J6, as seen at the left of the page. These are differential transmission lines from the computer matrix multiplexer. Each of the 10 line receivers convert an active low input to a positive level that is equivalent to a binary 1. Each of these receiver groups are fed to decoding indicators that decode and display the signals as seen on the conversion tables for 2, 3, and 4 input display units. These input conversion tables are located on sheet 4 of the referenced drawing.

(2) Hours/Minutes/Seconds Display Input Circuits. (See figure 7-8, sheet 4.) Time indicator inputs enter on J12 and J13. These are negative level, single ended inputs. Each input is passed through a level converter. As each input line rises from the negative level toward zero, the output of the level converter goes from zero toward positive. A positive signal is equal to a binary 1 on the input of the decoding indicators. The indicator displays are decoded as shown on the conversion tables on the logic diagram.

(d) System Alarm Inputs. (See figures 7-14 through 7-23.) Circuit diagrams are provided in section VII to show how the alarm circuits external to the somc are arranged. This information is useful for troubleshooting as well as an aid to understanding the alarm system.

2. Output Circuits. (Reference figure 7-8.)

(a) Dual Line Outputs. An example of dual-line, differential control output is on sheet 7 of the drawing, area GI, 2, and 3. This is the CPU PRIMARY SELECT A and B control. Note that as the control is thrown from one position to the other, the flip-flop, formed by the NAND gates 7H2A and 7G2A, is changed from one state to the other as pins 55 and 53 on board location A116 are alternately grounded. At the same time, lamps A and B are alternately furnished a ground. As the flip-flop changes states, the differential output driver networks 7H2B and 7G2B also change. Because the outputs of the flip-flop at pins 25 and 54 of A116 are always opposite, the outputs of the line drivers are opposite ensuring the selection of one cpu at a time. The outputs of these drivers are applied to pins v and w, s and t of J7. These two lines are connected to the computer select circuitry of the system control equipment.

(b) Single Line Outputs. Examples of single line outputs are seen on sheet 5 of the drawing. Locate areas BI, 2, 3, and 4 (CPU OFF-LINE B control circuit). Observe that switching the control from one position to the other causes ground to be applied to alternate inputs of the flip-flop formed by 5C3A and 5B3A. Alternating the ground from pin 26 of the flip-flop to pin 57 will cause it to change states. This change is coupled to the line driver, pins 27, 56, and 57. The line driver output is connected to pins p and q of J7.

(c) Alarm Outputs. An alarm output is provided to notify the computer should one of the five olm&t power supplies fail. On sheet 7 of figure 7-8, areas F1, 2, and 3, observe that the extended NOR gate 7F3A receives status information from each of the five power supplies on pins 11, 12, 13, 14, and 43 of board A114. Should any of these inputs drop, the output of 7F3A goes high. The output at pin 10 is connected to the inverting amplifier 7F3B and to the differential line driver network 7E2B. The output of 7F3B, pin 9 is connected to pin 46 of the lamp driver network 7F2A. A signal low at this point causes the transistor driver to conduct, connecting the olm&t error lamp to ground. The output of 7F3A, pin 10, is connected to pins 48, 49, and 18 of the line driver 7E2B. The output of this driver is applied to pins N and P of J7 which are connected to the computer.

3. Panel Functions. (Reference figure 7-8.)

(a) Audible Alarm Circuit. The left side of sheet 9 shows the terminal portion of the alarm collection circuitry terminating at the audible signal flip-flop input, pin 33 of board location A105. The audible alarm flip-flop is a latching device triggered by a signal low pulse which is formed by the pulse forming networks in each alarm line. When the latching flip-flop is set, the output (pin 32 of 9D6B) is a signal low. The output is connected to pin 50 of 9C6A, which is the audible alarm driver. Applying a signal low to the input of 9C6A causes a signal high to be applied to the base of the driving transistor, supplying ground to the audible alarm device 9C5A (DS74). The audible alarm is silenced by resetting the latching flipflip. If either the DISABLE ALARM SW or the SILENCE ALARM SW are closed, ground potential is applied to pin 31 to 9D6B. This drives the output of 9D6B high, cross couples to pin 2 of 9E6C and resets the flip-flop. Note that the audio alarm sounds when the lamp test is actuated.

(b) Lamp Test Circuit. (Refer to figure 7-8, sheet 10.) The circuitry displayed is a schematic diagram of the lamp test network and switch. Note that there is a blocking diode for each indicator on the somc control panel. This is necessary to enable the lamp circuit to be completed to ground through the LAMP TEST switch

Table 4-5. Monitor and Test Group Integrated Circuit Cross Reference

Integrated Circuit Type															Circuit Card Part No. 3300-	Locations Used	
U7B9615 59X	U7B9614 59X	U6B9615 59X	U6B9614 59X	U6A9625 59X	MC4024P	SN75450	SN74440	SN74430	SN74420	SN74410	SN74405	SN74404	SN74401	SN74400		Sig. Data Conv. Location 411A1	Somc Controller Location 217AB2
											x	x			44039	A7	
									x		x				44040	A8	
									x	x					44041	A9	
											x			x	44042	A10	
		x	x												44044	A2	
							x								46008		A102
														x	46012		A103, 105, 115, 116
												x			46013		A104, 106
								x							46017		A112, 113, 114, 123
x															46027	A1	A216, 217, 220, 221
	x														46028	A3, 4, 5, 6	A214, 219
					x							x	x		46075		A101
						x									46083		A201, 202, 203, 205, 206, 207, 209, 210, 215, 218
				x											46093		A222, 223, 224

without interaction with other circuits being tested. The +25-volt dc lamps are arranged in three groups for current division and the +5-voit dc lamps occupy one switch section. Note that connection is made to the audible alarm circuit during lamp test, causing it to be activated.

4-8. Integrated Circuit Descriptions.

The paragraphs that follow contain descriptions of integrated circuits used on custom made printed circuit cards for Countermeasures Receiving Sets AN/FLR-9(V7) and AN/ FLR-9(V8) monitor and test group. Experienced technicians are familiar with many of them, but all are included for completeness and reassurance. Refer to table 4-5 for cross reference between circuit part numbers and applicable manufacturer's integrated circuit type numbers.

a. SN7400 Quadruple Two-Input Positive NAND Gate. The SN7400 integrated circuit contains four identical two-input positive-logic NAND gates. The output of each such gate is at logic low only when both of its inputs are at logic high. If either input is low, output is high. Connections are shown in figure 4-15.

b. SN7401 Quadruple Two-Input Positive NAND Gate. The SN7401 integrated circuit contains four identical two-input positive-logic NAND gates with open-collector outputs. The output of each such gate is at logic low only when both of its inputs are at logic high. If either input is low, output is an open circuit. Connections are shown in figure 4-15.

c. SN7404 Hex Inverter. The SN7404 integrated circuit contains six identical signal inverters. The output logic level for each inverter is opposite its respective input logic level. Connections are shown in figure 4-15.

d. SN7405 Hex Inverter. The SN7405 integrated circuit contains six identical signal inverters with open-collector outputs. The output of each inverter is at logic low when its input is at logic high. When an inverter input is at logic low, its output is an open circuit. Connections are shown in figure 4-15.

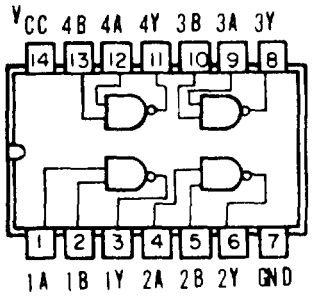
e. SN7410 Triple Three-Input Positive NAND Gate. The SN7410 integrated circuit contains three identical three-input positive-logic NAND gates. The output of each such gate is at logic low only when all of its inputs are at logic high. If any input is low, output is high. Connections are shown in figure 4-15.

f. SN7420 Dual Four-Input Positive NAND Gate. The SN7420 integrated circuit contains two identical four-input positive logic NAND gates. The output of each such gate is at logic low only when all of its inputs are at logic high. If any input is low, output is high. Connections are shown in figure 4-15.

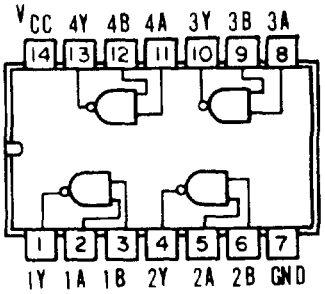
g. SN7430 Eight-Input Positive NAND Gate. The SN7430 integrated circuit contains an eight-input positive-logic NAND gate. The output of this gate is at logic low only when all eight inputs are at logic high. If any input is low, output is high.

Connections are shown in figure 4-15.

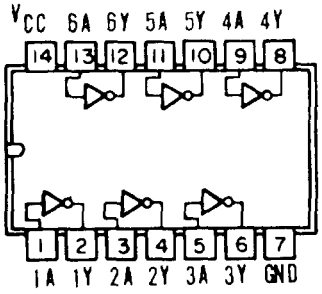
h. SN7440 Dual Four-Input Nand Buffer. (See figure 4-16.) The SN7440 integrated circuit contains two identical four-input positive-logic NAND gates designed to serve as buffers. The output of each such gate is at logic low only when all of its inputs are at logic high. If any input is low, output is high. Each gate has a normalized fan-out (drive) capability of 30, compared to 10 for non-buffer type integrated circuits. Connections are shown in figure 4-16.



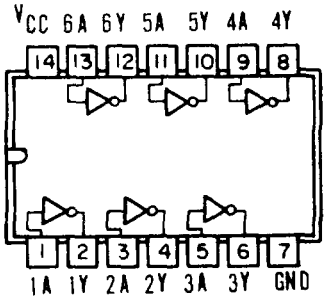
SN7400



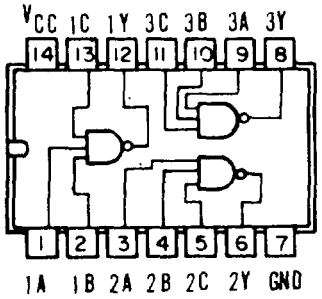
SN7401



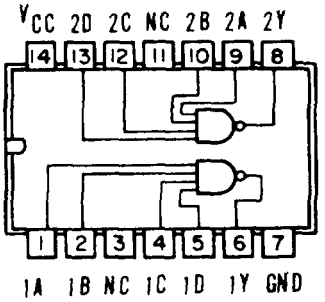
SN7404



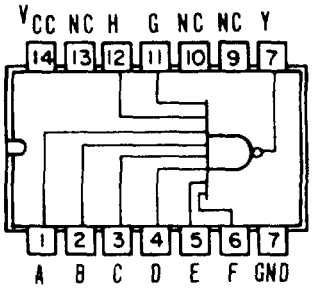
SN7405



SN7410



SN7420



SN7430

35699

Figure 4-15. Integrated Circuit Connections

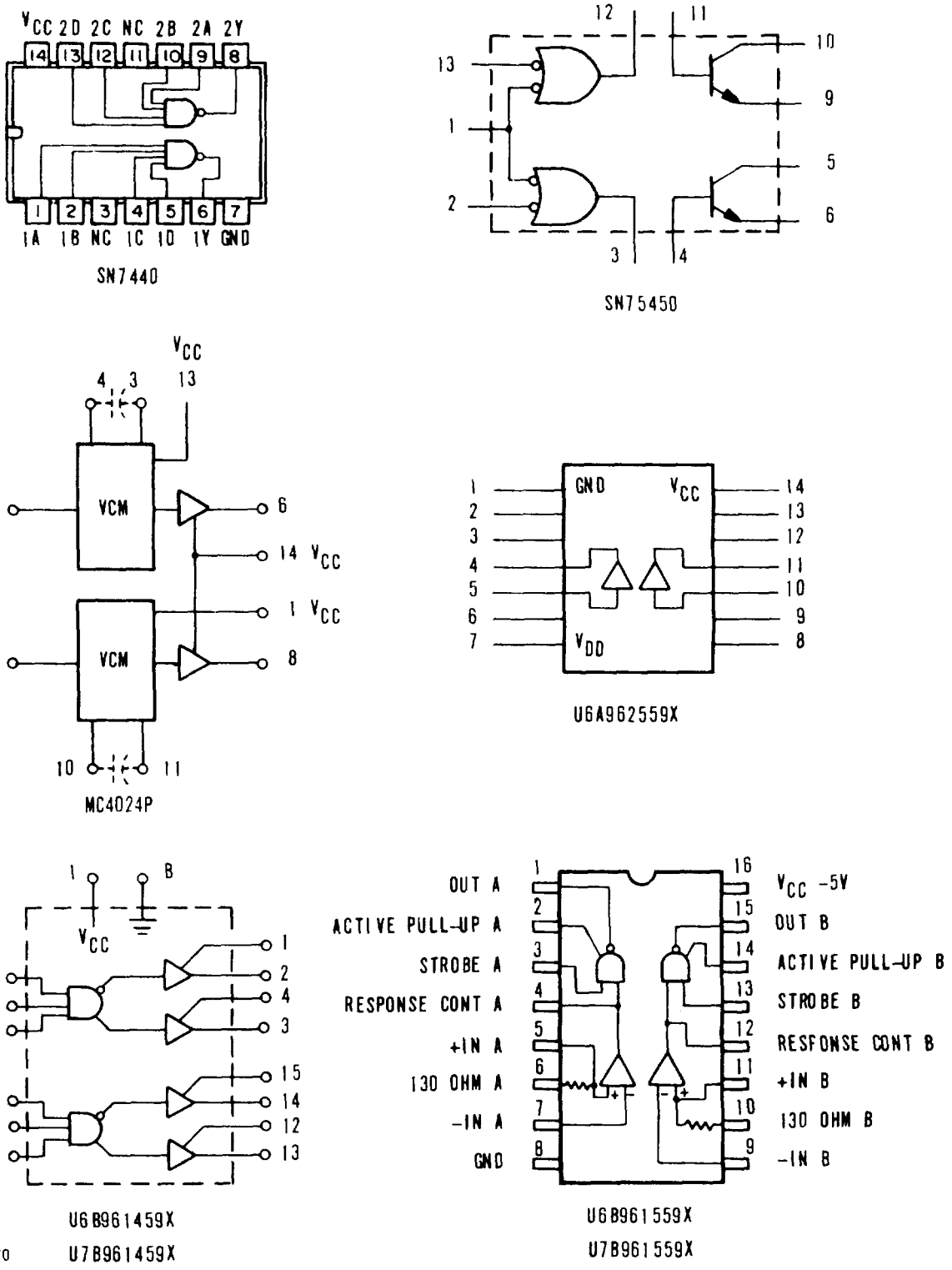


Figure 4-16. Integrated Circuit Connections

i. SN75450 Dual Lamp Driver. The SN75450 integrated circuit contains two positive logic NAND gates and two transistors. As shown in figure 4-16, one input to each NAND gate is combined. The output from a NAND gate is at logic high if either or both of its inputs is at logic low. If both inputs are high, output is low. All three connections for each transistor are available for emitter or collector loading, The NOR gate output is adequate for driving tie transistor to control a small indicator lamp.

j. MC4024P Voltage-Controlled Multivibrator. The MC4024P integrated circuit contains two identical and independent multivibrators. The frequency of each square-wave output is controlled by the voltage of a control signal. Frequency is variable over a 35-to-1 range; the range is determined by the size of an external capacitor. The value of the capacitor and upper and lower frequency limits are given by the equations:

$$C_{(f)} = \frac{500}{\text{Freq.}_{(\text{max, Hz})}}$$

and

$$C_{(f)} = \frac{100}{\text{Freq.}_{(\text{min, Hz})}}.$$

Maximum operating frequency is 25 MHz, and control voltage can be +1 to +5 volts dc. Each multivibrator is provided with a buffer to provide standard logic level outputs. Both buffers are operated from the same power input terminal. Each multivibrator operates from a separate power input terminal. Connections are shown in figure 4-16.

k. U6A962559X Dual MOS to CCSL Level Converter. The U6A962559X integrated circuit contains two identical signal level converters. Each converter provides a compatible current sinking logic (CCSL) level output in response to a metal-oxide semiconductor (MOS) logic input. Input impedance is high to prevent loading of driving MOS signal level. Connections are shown in figure 4-16.

l. U6B961459X Dual Differential Line Driver. The U6B961459X integrated circuit contains two identical circuits designed to drive long transmission lines in response to single-ended logic level inputs. As shown in figure 4-16, each identical circuit is provided with a three-input AND/NAND gate. When all three inputs are at logic high, the gate provides a complementary pair of signals which drive separate amplifiers. Each amplifier has two outputs, one for pull-up, the other for pull-down, to allow wired-OR function with single-ended or differential operation. Differential operation is accomplished by connecting the two outputs of each amplifier together.

m. U6B961559X Dual Differential Line Receiver. The U6B961559X integrated circuit contains two identical circuits designed to accept differential line signals and provide corresponding single-ended logic level signals. As shown in figure 4-16, line input to each receiver is to a differential amplifier. A line terminating resistor is available for external connection. Differential amplifier output is brought to a terminal and to an AND/NAND gate. Differential amplifier output, called response control, can be slowed down by connection of an external capacitor. A second input to the AND/NAND gate provides for strobe control of received data. When both of its inputs are high, the AND/NAND gate provides a complementary pair of outputs. One output is the open collector type. The second output, called active pullup, can be connected to the first output to provide discrete two-level logic output.

n. U7B961459X Dual Differential Line Driver. The U7B961459X integrated circuit contains two identical circuits designed to drive long transmission lines in response to single-ended logic level inputs. As shown in figure 4-16, each identical circuit is provided with a three-input AND/NAND gate. When all three inputs are at logic high, the gate provides a complementary pair of signals which drive separate amplifiers. Each amplifier has two outputs, one for pull-up, the other for pull-down, to allow wired-OR function with single-ended or differential operation. Differential operation is accomplished by connecting the two outputs of each amplifier together.

o. U7B961559X Dual Differential Line Receiver. The U7B961559X integrated circuit contains two identical circuits designed to accept differential line signals and provide corresponding single-ended logic level signals. As shown in figure 4-16, line input to each receiver is to a differential amplifier. A line terminating resistor is available for external connection. Differential amplifier output is brought to a terminal and to an AND/NAND gate. Differential amplifier output, called response control, can be slowed down by connection of an external capacitor. A second input to the AND/NAND gate provides for strobe control of received data. When both of its inputs are high, the AND/NAND gate provides a complementary pair of outputs. One output is the open collector type. The second output, called active pullup, can be connected to the first output to provide discrete two-level logic output.

SECTION V

MAINTENANCE AND REPAIR

5-1. Scope.

This section contains maintenance duties assigned to the operator and the unit repairman. Maintenance duties assigned to the operator consist primarily of preventive maintenance with limited troubleshooting and repair. Maintenance duties assigned to the unit repairman consist of preventive and corrective maintenance (including troubleshooting, repair, alignment, and adjustment) on equipment within the monitor and test group with checkout and repair of these equipments. Applicable illustrations are located at the end of this section.

5-2. Non-Maintenance Items.

Non-Maintenance items are defined as those items that are either repairable at the factory where they originated or are throw-away items. In either case, they are considered beyond the local repair capability. Non-maintenance items are identified on equipment illustrations by leader lines and appropriate note references.

5-3. Preventive Maintenance. (See table 5-1.)

Preventive maintenance is the systematic inspection and servicing of equipment to prevent breakdown. This maintenance is normally conducted on a regularly scheduled basis although some items may require care on a demand basis. Table 5-1 lists preventive maintenance procedures and recommended performance intervals.

Table 5-1. Maintenance Schedule

Period	Procedure
Daily	1. Run olm&t OSC TEST. 2. Check equipment general cleanliness. 3. Make sure that cooling air inlets and outlets are free of obstructions. 4. Check all controls and other items that are handled frequently to insure that are clean and in good repair. 5. Operate remaining three olm&t test controls long enough to determine that olm&t is operating properly.
Weekly	1. Clean air filter in somc 217. 2. Clean air filter in the frequency counter located in cabinet 411. This air filter is a fine mesh

Table 5-1. Maintenance Schedule (Continued)

Period	Procedure
	screen and must be checked regularly to prevent clogging. Clean and service as instructed in the frequency counter equipment manual. 3. Check blower fans internal to analog-to-digital converters located in rack 411. 4. Note that the screens on the rear of the analog-to-digital converters, located in cabinet 411, are exhaust screens. The air inlets are located in the bottom plate of the instrument.
Bi-weekly	Check and adjust olm&t equipment as instructed in paragraph 5-13.e.
Monthly	Check all power supply voltages as instructed in paragraph 5-13.
Semi-annually	Calibrate vector voltmeter, frequency counter, and analog-to-digital converter.

5-4. Maintenance Test Equipment (See table 5-2.)

Table 5-2 lists maintenance test equipment used for the monitor and test group.

Table 5-2. Maintenance Test Equipment

Type Designation	Nomenclature	Use
Signal Generator	Hewlett-Packard 606B	Used as signal source for equipment tests.
Multimeter	Simpson 260-5	Used to measure ohms, volts, and amperes in general troubleshooting of equipment.
Differential Voltmeter	Fluke 853A	Used to test and calibrate dc power supplies.
Differential Line Receiver Test Set 3300-48013	Analyzer Differential Signal output TS-3287/FLR-9(V)	Used to check outputs of signal data converter.
Differential Signal Simulator Test Set 3300-48005	Simulator Differential Signal SM-664/FLR-9(V)	Used to check vvm control circuit in signal data converter.

Table 5-2. Maintenance Test Equipment (Continued)

Type Designation	Nomenclature	Use
		Used to check computer command input circuits and control output circuits in somc. Used to manually command switch closure in A, B, and C olm&t matrices.
Single-Ended Signal Simulator Test Set	Simulator Single-Ended Signal SM-665/FLR-9(V)	Used to check alarm circuits in somc.
Test Cable Assembly	Cable Assembly Set, Test MX-9329/FLR-9(V)	Test cables from this assembly are used for interconnecting test equipment items referenced in the troubleshooting and calibration procedures.

5-5. Special Maintenance Tools.

No special maintenance tools are used for the monitor and test group.

5-6. Corrective Maintenance.

Corrective maintenance is the efficient location and repair of a malfunction. In this case, corrective maintenance begins at the monitor and test group level that includes all eight equipment racks in the central and the operations buildings. The equipment level of maintenance is the next step in trouble isolation and covers functional units such as panel assemblies and power supply assemblies. The module level of maintenance is to isolate a malfunction to a certain circuit board or other replaceable module. Repair of circuit boards is described in the Card Repair Manual, TM 32-5895-239-15. Refer to applicable manual listed in table 1-6 for maintenance of commercial equipment.

5-7. Logical Troubleshooting Procedures.

a. General. Initial steps in the troubleshooting of a computer-controlled group, such as monitor and test, begin with analysis of the alarm indication and computer readout that accompany the malfunction. Analysis of these indicators leads to the offending equipment and further systematic checks lead to the replacement of the circuit board or part that has failed.

b. Sectionalization. The monitor and test group generally consists of three functional areas. These are signal generation and insertion, signal retrieval and measurement, and the somc area. Fault isolation to one of these areas is the first step in troubleshooting the monitor and test group.

1. Visual. (Refer to paragraph 3-2). Examinations of the indicator on the somc control panel, the panel meter on the vector voltmeter (rack 411), and the registers on the analog-to-digital converters (rack 411) are used with the tty printout for trouble isolation.

2. Operational. Analysis of the olm&t test results printed by the tty plus systematic checks in a functional area or equipment comprise the troubleshooting procedure.

c. Localization. After the malfunction has been traced to a functional area, it is isolated to an equipment. If the equipment is made of multiple assemblies, such as a matrix, the trouble is further isolated to an assembly. In some cases, however, the analysis is sufficient to go directly to a plug-in module. The equipment may be replaced by a standby equipment at this point or the trouble may be isolated further.

d. Isolation. In an equipment, the trouble is further isolated to a plug-in board or component. At this level, the decision is made to repair or replace the faulty assembly or component. Isolation of a trouble on a circuit board would proceed according to instructions in the card repair manual.

5-8. Group Level Operational Tests.

When trouble has been traced to the monitor and test group using system level test procedures or other indications, further tests are made. Operational tests that are used to check areas of the monitor and test group are the olm&t test select controls described in section 3. Simplified block diagrams shown in section 4 and the overall schematic shown in section 7 can be used for logical trouble isolation. The olm&t tests are the beamformer, antenna, switch matrix, and oscillator tests. The program cycles through these tests in this order if the test controls are activated. Any test control that is not set is skipped. A test remains activated as long as the control is set. Releasing a control (by pressing it again) resets that test to the beginning. A lengthy test can be halted and resumed without being reset to the beginning if the OLM&T FAULT is set to halt the test in progress.

NOTE

Setting the OLM&T FAULT Control causes all olm&t tests to be ignored, including path verification. This means that all switch paths connected during the period are connected without performing path verification testing. This can result in use of faulty switchpoints and signal path degradation. If the OLM&T FAULT is set for an appreciable time, the somc operator can determine the faulty switch paths in use by initiating an RFSM X-PT test immediately after resetting the OLM&T FAULT switch and allowing it to run until the path connection fault portion of the test has been completed.

Resetting the OLM&T FAULT control resumes the test at the point of interruption.

a. Oscillator Test. (See table 5-3.) Pressing the OSC TEST control tests the frequency of each of the 18 reference oscillators. Tty printouts are described in

message reference numbers (messages) 8 through 11. For a band, oscillator number, and frequency cross reference, see table 4-4.

b. beamformer Test. (See table 5-3.) Pressing the BEAM FORM control initiates the beamformer test cycle. At the beginning of each cycle, message 12 is output and the program performs an olm&t system test and a test signal interference test.

1. The olm&t test involves three reference paths (one per band) through the olm&t network only. The paths are checked

with the selected test oscillator in each band. The tty printouts associated with the olm&t self-test are messages 13 through 17.

2. The test signal interference test is performed next. Message 18 is printed to identify the selected oscillator for each band.

3. The actual beamformer test is performed next and uses messages 19 through 33. This portion of the beamformer test is dedicated to the antenna group. It can be allowed to run for 30 seconds or until the operator has seen enough to determine the condition of olm&t test circuits.

c. Antenna Test. (See table 5-3.) Pressing the ANT TEST control causes message 34 to be printed. This test also is preceded by the interference test and uses the same network as the beamformer test except that the test signal is injected into the outgoing port of the directional coupler using the other half of the group A test select matrix. This results in messages 35 through 37 being printed. This test is again allowed to run long enough to satisfy the operator that the olm&t equipment involved is operational or faulty.

d. Switch Matrix Test. (See table 5-3.) The switch matrix test uses all portions of the monitor and test equipment except the frequency meter. In this test, the group C matrix is utilized to sample the outputs of the switch matrix. This output is checked against amplitude tolerances. Pressing the RFSM X-PT control causes message 38 to be printed. The switch matrix test is preceded by an interference test which checks the omni beam in each band for interference at the frequency of the oscillators previously selected. If noise is present, the oscillator number is incremented by one until a satisfactory test is possible. The accepted oscillator numbers are then printed. The switch matrix testing begins with a check of all currently in-use paths. Faults detected result in a tty PATH CONN FLT message and a FAULT indication to the mission operator position. The test then proceeds to check the unused switchpoints in the Al and A2 levels of the switch. If the olm&t PRINT is also activated, the tty begins printing message 43. If trouble is detected, messages 39 through 42 and message 44 may be printed. Message 45 notifies the operator that the test is complete. This test would normally run approximately 30 minutes if it were allowed to cycle through. Run the test long enough to determine if a suspected problem exists in the olm&t group C matrix. A fault in the group C matrix is identified by message 6. To determine if message 6 signifies a true switchpoint fault or a group C matrix fault, use the tty to perform a single path test using the suspected Al input port with an output other than that identified in the fault message. If the test results in no failure, the Al input is not at fault. Refer to CM 32-5895-237-14 for troubleshooting procedures for the group C matrix.

e. Path Verification Tests. (See table 5-3.) Unless inhibited, a path verification test is performed on each switch path selected by a beam selector unit. Testing is accomplished in much the same manner as during RFSM switchpoint testing

described in paragraph 5-8.d. Switchpoint failures detected during path verification testing result in a tty print of message 1, followed by message 2, 3, 4, 5, 6, or 7. Switch path blocking occurs concurrent with fault messages 3 and 5. When switch blocking occurs, the switch card identified by the fault message is logged out by the computer and is disregarded in subsequent switch path decisions. The switch card may be returned to use (logged in) by typing the command PURGE on the tty. This returns all previously blocked switch cards to use during switch path selection.

f. Path Verification and X-PT Message Variations. (Refer to messages I through 6 and 39 through 42.) Path verification messages have priority over the olm&t testing and may appear during the X-PT testing readout. The fault messages which result during X-PT testing contain the word TEST whereas path verification messages do not.

g. Individual Olm&t Tests. (Refer to Section III, Operation.) Individual tests to check a certain function in the olm&t circuits using tty inputs are described in the AN/FLR-9(V8) Set Manual IM 32-5895-231-15/1 or the AN/FLR-9(V7) Set Manual IM 32-5895-231-15.

Table 5-3. Tty Troubleshooting Message Formats

Message Reference Number	Message	Code	Remarks
1	PATH VER FAILURE OPER XXX, RCVR Y BEAM ZWW	X is operator number Y is receiver 1 or 2 Z is band W is beam number	This message is the result of a test signal which is out of limits on a path selected in response to a beam request from an operator. It is followed immediately by one of the messages 2 through 6 explaining the nature of the fault.
2	A3 XPT FLT ID: XXX,YY,ZZZ	X is switch matrix input pin number Y is switch matrix A2 submatrix number Z is switch matrix output pin number	This message identifies a bad crosspoint in an A3 submatrix. In order to determine this, the program has obtained a good test signal by using an alternate crosspoint on the same input line of the A3 submatrix. This is the first step in fault isolation. Fault isolation is terminated as soon as a fault can be identified. A fault light and blank display is received by operator.

Table 5-3. Tty Troubleshooting Message Formats (Continued)

Message Reference Number	Message	Code	Remarks
3	A2 XPT/A3 INPUT FLT ID: XXX,YY,ZZZ	X is switch matrix input pin number Y switch matrix A2 submatrix number Z switch matrix output pin number	This message identifies a bad path from the A2 stage to A3 stage. This can be either a bad A2 crosspoint or a bad input line to A3. To determine this, the program has used an alternate crosspoint on the A2 stage input line of the original path. This injects the test signal into an alternate A3 submatrix also. This is the second step in fault isolation. This message results in blocking of an A3 input line if there is no coupling (refer to message 48). An alternate path is requested when there is no coupling. If there is coupling, a fault light and blank display signal is sent to the operator who requested the beam and message 4 is output.
4	COUP IN A3 - NO ALT PATH		This message follows a path verification failure message when coupling in the A3 level exists and no alternate path is available. Coupling means that the requested path (A3 input line) is in use by another operator in the same A3 submatrix using the same beam as the requested beam. Therefore, even though the current test shows that path to be faulty, no block is placed on the A3 input line.

Table 5-3. Tty Troubleshooting Message Formats (Continued)

Message Reference Number	Message	Code	Remarks
5	A1 XPT/A2 INPUT FLT ID: XXX,YY,ZZZ	X is switch matrix input pin number Y switch matrix A2 submatrix number Z is switch matrix output pin number	This message identifies a bad path from the A1 stage to A2 stage. This can be either a bad Al crosspoint or a bad A2 input line. In order to determine this, the program has tested a path through an alternate A2 submatrix to the original output pin requested. The alternate path to the operator is retained if it tests good and the beam is displayed to the operator. No fault light is sent to the operator.This message results in blocking of the original A2 input line (see message 48).
6	A1 INPUT FLT ID: XXX,YY,ZZ	X is switch matrix input pin number Y is switch matrix A2 submatrix number Z is switch matrix output pin number	This message identifies a bad path into the A1 stage. This implies a bad input line in the A1 stage. In order to determine this, the program has found all paths through the switch bad but the olm&t signal is good. Note that an olm&t group C failure would also exhibit this result. This message does not result in any blocking in the switch or an alternate path request. A fault light and blank display signal is sent to the requesting operator.
7	OSC LEV FLT - PATH VER VOID		This message indicates that a problem exists in the olm&t network or the amplifier/power divider/beamformer network. There is no switch blocking in response to this message. A fault light is displayed to the operator along with the azimuth display to show that

Table 5-3. Tty Troubleshooting Message Formats (Continued)

Message Reference Number	Message	Code	Remarks
			olm&t was not able to verify the path. The path is given to the operator. A succession of these printouts is an indication that the A or B group matrix is faulty. Conducting a single beamformer test on the beam identified by the input pin number may assist in determining the source of the problem.
8	OLMT OSC TEST START		This message is printed each time the oscillator test starts. It is followed by a day of year, time of day printout. (This test tests all test oscillator frequencies for tolerance.)
9	OSC XX FREQ FAULT REF YYYYYYYY TOL ZZ FREQ WWWWWWWW	X is oscillator number 1-18 Y is reference frequency Z is tolerance W is measured frequency	This message is printed for each oscillator with frequency which is out of tolerance.
10	OSC XX FREQ YYYYYYYY	X is oscillator number 1-18 Y is frequency in Hz	This message is printed if the PRINT button is activated at the somc during the oscillator test.
11	OLMT OSC TEST FINISHED		This message is printed each time the oscillator test completes a cycle.
12	OLMT BMFR TEST START		This message is printed each time the beamformer test is activated. It is followed by a day of year, time of day printout.
13	TEST CABLES OK		This message is printed if the reference paths are OK. It is an indication that olm&t is functioning properly.
14	TEST CABLE FAULT-BAND X	X is band A, B, or C	This message is printed whenever one of the reference

Table 5-3. Tty Troubleshooting Message Formats (Continued

Message Reference Number	Message	Code	Remarks
			cables is out of tolerance. It is followed immediately by message 15 or 16.
15	REF XXX.X TOL Y.Y AMP ZZZ.Z	X is reference amplitude in millivolts Y is tolerance allowed in millivolts Z is measured amplitude in millivolts	
16	REF *XX.X TOL YY.Y PHS +ZZ.Z	X is reference phase in degrees Y is tolerance allowed in degrees Z is measured phase in degrees	These messages give the parameters of a failure. Low amplitude readings may be assumed to be 0 because the voltmeter measures noise.
17	TEST CABLE X AMP YYY.Y PHS ZZZ.Z	X is band Y is amplitude millivolts Z is phase degrees	This message appears if PRINT button is activated during cable test. The test signal interference test is performed by connecting the vector voltmeter to an omni beamformer at the frequency of a selected test oscillator and measuring the signal present. If the signal exceeds the interference limit, then the test oscillator number for that band is incremented automatically by one and the test repeated. If interference is present at all test frequencies in a band, the originally selected oscillator is used and INT OSC XX is output where XX is the original oscillator number. Message 18 appears once for each band indicating which oscillator was used.

Table 5-3. Tty Troubleshooting Message Formats (Continued)

Message Reference Number	Message	Code	Remarks
18	OSC xx	X is oscillator number 1-18	Output message identifying oscillator in use. Listed once for each band at the beginning of RFSM X-PT, antenna, and beamformer tests. Also, an input command used to select the oscillator to be used for olm&t testing (when followed by a carriage return).
19	BMFR FAILURE - BAND X BEAM Y	X is band number Y is beam number	This message identifies a beamformer to which a fault has been isolated. This is done by connecting the amplifier/ power divider used in the original test through an alternate beamformer. If test is good, it implies that the original beamformer network has a problem and is identified by the message. If the second test is also bad, it implies that the amplifier/power divider network has a problem and message 20 rather than 19 appears. Note that the olm&t network is considered good after the reference cable test. This message is followed by message21, then 15 or 16.
20	AMP/PWR DIV FAILURE - BAND X ANT YY	X is band number Y is antenna number	This message is followed immediately by message 21.
21	BAND X BEAM YY PORT ZZ FAULT	X is band number- Y is beam number-x Z is beamformer port number being tested	This identifies the test path which resulted in the fault. This message is followed immediately by message 15 or 16 which identifies the type of fault and ,values involved.

NOTE

A bad power divider or amplifier can affect the test results of 8 or 16 paths. This results in a series of fault messages through one test cycle. The test cycle includes each of the alternate antenna element signal paths

Table 5-3. Tty Troubleshooting Message Formats (Continued)

Message Reference Number	Nomenclature Message	Use Code	Remarks
	NOTE (Continued) **through the beamformers. To avoid tying up the teletype with redundant messages, four shorthand messages have been devised to identify these alternate path failures. These appear after the complete fault message has been presented once for each cycle. See paragraphs 5-7.e.3.(b) and (c) in the V7 or V8 set manuals.**		
22	BM XX AM	Shorthand	This message corresponds to messages 19 and 15.
23	BM XX PH	Shorthand	This message corresponds to messages 19 and 16.
24	ANT XX AM	Shorthand	This message corresponds to messages 20 and 15.
25	ANT XX PH	Shorthand	This message corresponds to messages 20 and 16.
26	MONI BEAM XX BAND Y	X is beam number Y is band number	This message results if the PRINT button is activated during beamformer test. It appears as each new beam is tested. It is followed by message 27.
27	ANT XX PHS ZZZ.Z AMP YYY.Y	X is antenna number Y is measured amplitude in millivolts Z is measured phase in degrees	This message appears 16 times for each beam in bands A and U and 8 times for band C (when the PRINT control is activated.)
28	BAND X OMNI PORT YY FAULT	Y is antenna number for the omni input	This message appears whenever an omni beamformer measurement is out of tolerance. No fault isolation is done on omni beamformers. The message is followed immediately by message 15 or 16 identifying the fault.

Table 5-3. Tty Troubleshooting Message Formats (Continued)

Message Reference Number	Message	Code	Remarks
29	OMNI BEAM BAND X	X is band A, B, or C	This message appears at the beginning of each omni beam tested if the PRINT button is on. Message 27 follows a total of 48 times for bands A or C, or 96 times for band B.
30	BAND X SECT Y ANT ZZ FAULT	X is band A, B, or C Y is sector beam number 1-3 A is antenna number	The sector beamformer test follows the omni beamformer test. This message identifies a fault in a sector beamformer test. No fault isolation is done on a sector beamformer. This message is followed immediately by message 15 or 16 which identifies the fault.
31	SECT BEAM X BAND Y	X is sector beam number 1-3 Y is band A, B or C	This message appears at the beginning of a sector beamformer test when the PRINT button is on. It is followed by message 27 as in monitor and omni tests. There are four antennas in a band A sector beam, three in band B, and two in band C.
32	AMP TOL X.X PHS TOL Y.Y	X is amplitude tolerance in millivolts Y is phase tolerance in degrees	This message appears at the end of each monitor, omni or sector beam test result if the PRINT control is activated.
33	OLMT BMFR TEST FINISHED		This is the beamformer test conclusion message.
34	OLMT ANT TEST START		This is the start message for the antenna test. It is followed by a day of year, time of day printout, and oscillator identification numbers. Refer to message 18.

Table 5-3. Tty Troubleshooting Message Formats (Continued)

Message Reference Number	Message	Code	Remarks
35	ANT X YY FAULT	X is band Y is antenna number	This message identifies a fault in an antenna. This is determined by outputting to the test antenna and measuring the reflected signal at the beamformer output of the monitor beam which uses the element under test as a boresight input. Message 35 is followed immediately by message 15 identifying the fault.
36	ANT TST X YY AMP ZZZ.Z	X is band Y is antenna number Z is measured amplitude in millivolts	This message results when PRINT button is on during antenna test. The antenna test cycles through each antenna in each band once.
37	OLMT ANT TEST FINISHED		This is the antenna test conclusion message.
38	OLMT RFSM TEST START		This is the start message for the RFSM test. It is followed by a day of year, time of day printout and oscillator identification numbers. The OLMT RFSM test is designed to test all the crosspoints in the A1 and A2 stages of the switch matrix. It uses only the last output pin (10) in any A3 submatrix for an output port. The reason for this is to prevent breaking a beam in use in the A3 stage. The test requires approximately 30 minutes to cycle once if there are no error message printouts. When an error is detected, message 39, 40, 41, or 42 is printed out. These messages are very similar to the path verification error messages,

Table 5-3. Tty Troubleshooting Message Formats (Continued)

Message Reference Number	Nomenclature Message	Use Code	Remarks
			and the fault isolation procedure is identical. Reference is made to the path verification messages in explaing these. No blocking is done in the switch as a result of the OLMT RFSM test.
39	A2 XPT/A3 INPUT TEST FLT ID: XXX,YY,ZZZ	X is switch matrix input pin number Y is switch matrix A2 stage submatrix number Z is switch matrix A3 submatrix output pin number	This message is analogous to message 3.
40	A1 XPT/A2 INPUT TEST FLT ID: XXX,YY,ZZZ	Same as 39	This message identifies a bad path from the A1 stage to A2 stage. This can be either a bad A1 crosspoint or a bad A2 input line. In order to determine this, the program has tested a path through an alternate A2 submatrix to the original output pin requested. This message is analogous to message 5.
41	Al INPUT TEST FLT ID: XXX,YY,ZZZ	Same as 39	This message is analogous to message 6 except no fault light is sent to operator.
42	OSC LEV FAULT - INVALID RFSM TEST		This message is analogous to message 7 except no fault light is sent to operator.
43	RFD PATH: XXX,YY,ZZZ REF UUU.U TOL VV.V AMP WWW.W	X is switch matrix input pin number Y is switch matrix A2 submatrix number Z is switch matrix output pin number U is reference amplitude in millivolts V is tolerance in millivolts. W is measured amplitude in millivolts	This message is written if the PRINT control is set during the RFSM test.

Table 5-3. Tty Troubleshooting Message Formats (Continued)

Message Reference Number	Nomenclature Message	Use Code	Remarks
44	PATH CONN FLT OPER XXX,Y BEAM Z WW	X is BSU position number Y is receiver number Z is band A, B, or C W is beam number	This message identifies an in-use path which fails the RFSM test. No action occurs other than lighting the FAULT lamp on the affected beam selector unit.
45	OLMT RFSM TEST FINISHED		End of test.
46	EOC FAULT		End-of-conversion signal output from either analog-to-digital converter has not been received by computer. This is a warning that the vector voltmeter (vvm) has not been properly set up by the signal data converter before reading. Testing of an improperly specified sector beam or an attempt to test a df beam causes this message to be typed. This message does not cause a computer halt nor is olm&t ignored.
47	VV LOCK		This message is output when the vvm fails to notify the computer that automatic phase lock has been accomplished before the test data has been accepted by the cable scanner. This means that either the vvm is defective, or the signal data converter has failed. This message does not cause a computer halt nor is olm&t ignored. Testing of an improperly specified sector beam or an attempt to test a df beam causes this message to be be typed.
48	AX BLOCKED	X is the stage number (1 or 2)	This message occurs in response to a single path test of the switch matrix when a requested crosspoint in either the A1 or A2 stage is in use.

Table 5-3. Tty Troubleshooting Message Formats (Continued)

Message Reference Number	Message	Code	Remarks
49	AZ BLOCKED - PATH VER VOID		Output when path verification cannot be completed due to blocking.
50	SWITCH BLOCK AT PORT $XXX		Output when a requested beam or the adjacent beam on either side cannot be connected to operator due to blocking caused by path verification failures.
51	ILLEGAL FORMAT		This message is printed when the input command does not agree with specified format.
52	ILLEGAL SOMC INPUT		Output when an illogical input is received from somc due to hardware failure or improper procedure.
53	SOMC CONTROL		Output to acknowledge computer handover initiated by somc.
54	PATH VER OUT	Input message	Used to delete path verification only and retain the rest of the olm&t functions. Type PATH VER IN to restore path verification.
55	STAGE X SUBMATRIX YY OUTPUT ZZ REMOVED	Limits X = I or 2 Y = 1-16 or 1-19 Z = 1-19 or 1-40 (V7) Z = 1-19 or 1-80 (V8)	This tty command causes the computer program to flag the identified switch card and prevent its use in any subsequent path decisions. In addition, all operators currently using this switch card have their paths erased from the path-in-use table in memory. This means that subsequent beam requests from other operators can cause the path to these affected operators to be broken. Upon reselection, the affected operators would regain the requested beam through a separate path if available. At site V7,

Table 5-3. Tty Troubleshooting Message Formats (Continued)

Message Reference Number	Message	Code	Remarks
			a FAULT light is sent to the affected operators. In the event of path failure after path verification, when there is coupling which prevents other operators from gaining the affected beam, this command can be used to remove the coupling condition. After the condition is removed, the stage replaced command should be used to restore the switch card to use in memory.
56	STAGE X SUBMATRIX YY OUTPUT ZZ REPLACED	Limits X = 1 or 2 Y = 1-16 or 1-19 Z = 1-19 or 1-40 (V7) Z = 1-19 or 1-80 (V8)	This tty command causes the computer program to remove the flag from the switch card identified, and restore it for use in subsequent path computation decisions. If a switch card is identified which has not been flagged, the tty returns an ILLEGAL FORMAT message.
57	PURGE		This tty command causes the computer to remove the blocking flags from all switch cards which have been identified by the stage removed command or the path verification error detection routine.
58	STK	Stack message	This message results if more than two path verification failures occur in the time frame of one path verification failure message. System response time is limited by the tty printout speed. Too many messages result in this abbreviated message.

-9. Group Level Troubleshooting. (Refer to table 5-4.)

The purpose of group level troubleshooting is to isolate a malfunction to an equipment. At this stage, the results of tests made in paragraph 5-8 have been examined and all symptoms observed. Figure 7-5 is used with the symptoms to help localize troubles. Refer to table 1-5 and figures 1-2, 1-3, 1-4, and 1-5 for location of equipment.

Table 5-4. Monitor and Test Group Troubleshooting Chart

Item	Symptom	Cause	Remedy
1	Somc indicators HOURS, MINUTES, and SECONDS all read zero.	Loss of -7 volts dc to indicator units	Check fuse F1 at 217 AB5. Check power supply at 217 A3. Repair or replace. See item 1, table 5-5.
2	Somc indicators DAY OF YEAR, HOURS, MINUTES, SECONDS, and all status indicators extinguished. No computer control from somc.	Loss of +5 volts dc to somc	Check fuse F2 at 217 AB5. Check power supply at 217 AB4. Repair or replace. See item 2, table 5-5.
3	Somc indicators extinguished. Lamp test does not work.	Loss of +25 volts to somc	Check fuse F3 at 217 AB5. Check power supply at 217 AB4. Repair or replace. See item 3, table 5-5.
4	Any indicator on the somc control panel fails to illuminate.	Defective lamp	Press LAMP TEST to verify. Replace defective lamp. See item 4, table 5-5.
5	All switch path verification test show faulty path. test RFSM X-PT shows all bad. All other tests are good.	No output from group C matrix Olm&t	Repair group C matrix (refer to Reed Switch Matrices manual CM 32-5895-237-14). Refer to table 5-5.
6	Refer to item 5, with the following exception add: OLM&T POWER SUPPLY indicators OPS 2035V, 8V and/or 24V are illuminated.	Loss of power to group C matrix	Check fuse F1 at power supply assembly rear, 203A11. Check affected power supply at 203A11. Repair or replace. Refer to table 5-3. See item 5, 6, or 7, table 5-5.
7	Olm&t does not respond to test request. OLM&T POWER SUPPLY RH414 5V	No power supply output to group A and group B matrices	Repair or replace power supply at 414 A3. Refer to table 5-4. Refer to item 8 or 9, table 5-5.

Table 5-4. Monitor and Test Group Troubleshooting Chart (Continued)

Item	Symptom	Cause	Remedy
	and/or RH414 8V alarms are illuminated. is illuminated.	OLM&T ERROR	
8	Olm&t does not respond to test requests.	No input from matrix multiplexer Refer to table 5-3.	Refer to System Control Group manual IM 32-5895-233-15.
9	Same as item 8.	Output is not being read by cable scanner.	Same as item 8.
10	Same as item 8.	OLM&T FAULT control is set.	Release control.
11	All test oscillators in a band fail tests.	Oscillator power supply ply in the affected test oscillator assembly at rack	Check oscillator power sup- 413 location A1, A2, or A3. Refer to table 5-3, messages 9 and 10. Refer to table 5-5, item 10.
12	A single test oscillator fails tests.	*Oscillator defective.	Replace oscillator. Refer to table 5-3, messages 9 and 10. See figures 7-17, 5-6, 5-7, and 5-8.
13	All olm&t tests check bad.	No oscillator inputs to test circuit.	Bad group A matrix. Repair matrix. Refer to Reed Switch Matrices manual CM 32-5895-237-14. Refer to table 5-3, messages 13 through 18.
14	All olm&t tests check bad.	Defective group B matrix	Verify by manually selecting input probe A on the VVM to see if the normal oscillator reference voltage level from the group A matrix is present. Repair group B matrix. Refer to Reed Switch Matrices manual CM 32-5895-237-14. Refer to table 5-3.
15	A11 olm&t tests fail phase check.	Defective VVM H16-8405A or oscillator circuits.	Repair, replace, or readjust. Refer to table 5-3. Refer to vendor manual Hewlett-Packard Voltmeter CM 32-6625-240-14.

*Non-maintenance item, factory repairable

Table 5-4. Monitor and Test Group Troubleshooting Chart (Continued)

Item	Symptom	Cause	Remedy
16	Same as step 15, except OSC TEST fails frequency test (no input to frequency meter).	*Defective power combiner HY3 411 A3). 5-3, messages 9 and 10.	Replace combiner (located Refer to table
17	Same as item 16.	Defective variable attenuator olm&t.	Replace or readjust attenuator (located front panel of signal data converter 411A1).
18	Same as item 16.	*Defective power divider HY2	Replace divider (located 411A3).
19	No voltage level or phase readings are being output from olm&t. Tty types out VV LOCK.	Vvm failure	Repair or replace. Refer to Vvm manual for H16-8405A (CM 32-6625-240-14). Refer to table 5-3, message 47.
20	Olm&t output is missing either voltage level or phase readings. Tty types out EOC FAULT.	Analog-to-digital converter failure	Examine registers on converter front panels to see which one is defective. Repair or replace. Refer to analog-to-digital converter manual 52100T (CM 32-5820-241-14). Refer to table 5-3, message 46.
21	A11 olm&t test check bad except OSC TEST.	*Defective power combiner HY4	Replace combiner (located 411A3). Refer to table 5-3. See figure 5-2.
22	Same as item 21.	*Defective power divider HY]	Replace divider (located 411A3). See figure 5-2.
23	All olm&t tests fail frequency test. (Voltage and phase tests are normal.	Defective frequency counter	Repair or replace. Refer to frequency counter manual Hewlett-Packard Counter H33-5245M (CM 32-6625-239-14. Refer to table 5-3.
24	All olm&t tests fail. Vvm does not range on PROGRAM setting. Tty outputs VV LOCK.	Defective signal data converter power supply part number 3300-44037	Repair or replace. Refer to table 5-5, item 11.

*Non-maintenance item, factory repairable

Table 5-4. Monitor and Test Group Troubleshooting Chart (Continued)

Item	Symptom	Cause	Remedy
25	Tty outputs EOC FAULT.	Defective analog-to-digital converter	Repair or replace. Refer to table 5-3, message 46. Refer to analog-to-digital converter manual CM 32-5820-241-14.
26	Tty outputs VV LOCK	Defective vvm	Repair or replace. Refer to table 5-3, message 47. Refer to vvm manual H-16-8405A (CM 32-6625-240-14.)
27	Same as item 26 or any other single circuit indication normally prepared by the signal data converter.	Defective signal data converter circuit	Repair equipment. Refer to tables 5-6, 5-7, and 5-8.
28	All olm&t tests in one band check bad except OSC TEST.	*Defective bandpass filter	See figure 5-1. located 412A1, A2, and A3. Replace filter.

*Non-Maintenance item, factory repairable.

5-10. Equipment Level Operational Tests. (See tables 5-5 through 5-9.)

Equipment level operational test procedures given in table 5-5 are intended to supplement those tests in table 5-4. Information gained is used in equipment level troubleshooting. (See table 5-6, 5-7, 5-8, and 5-9.)

Table 5-5. Equipment Level Operational Tests

Item	Symptom	Cause	Remedy
1	Somc power supply AT 217A3 has no output voltage (-7 volts dc). (From item 1, table 5-4.)	Power supply LM258 inoperative. (See figures 5-15 and 5-18.)	Refer to Lambda Power Supply manual LM258 CM 32-6130-213-14.
2	Somc power supply AT 217AB4 has no output voltage (+5 volts dc). (From item 2, table 5-4.)	Power supply LM-E-5 inoperative. (See figures 5-15 and 5-17.)	Refer to Lambda Power Supply manual LM-E-5 CM 32-6130-214-14.

Table 5-5. Equipment Level Operational Tests (Continued)

Item	Symptom	Cause	Remedy
3	Somc power supply AT 217AB4 has no output voltage (+25 volts dc). (From item 3, table 5-4.)	Power supply LM-EE-28 inoperative. (See figures 5-15 and 5-17.)	Refer to Lambda Power Supply manual LM-EE-28 CM 32-6130-210-14.
4	Somc indicator does not illuminate during lamp test. (From item 4, table 5-4.)	Defective lamp	Replace lamp by grasping the indicator lens at top and bottom and working the lamp mounting block straight outward. Replace lamp. Replace lamp assembly. To replace lamp in DAYS/HOURS/MINUTES/SECONDS indicator assembly. (Refer to figure 5-19 and paragraph 5-12.)
5	Group C matrix power supply number 3 assembly has no +24-volt dc output. (From item 6, table 5-4.)	Defective power supply LM-B-24. (See figure 5-10.)	Refer to Lambda Power Supply manual LM-B-8 CM 32-6130-211-14.
6	Group C matrix power supply number 3 assembly has no +8-volt dc output. (From item 6, table 5-4.)	Defective power supply LM-EE-8. (See figure 5-10.)	Refer to Lambda Power Supply manual LM-EE-8 CM 32-6130-210-14.
7	Group C matrix power supply number 3 assembly has no +5-volt dc output. (From item 6, table 5-4.)	Defective power supply LM-B-5. (See figure 5-10.)	Refer to Lambda Power Supply manual LM-B-5 CM 32-6130-211-14.
8	Groups A and B matrix power supply number 1 has no +8-volt dc output. (From item 7, table 5-4.)	Defective power supply LM-CC-8. (See figure 5-11.)	Refer to Lambda Power Supply manual LM-CC-8 CM 32-6130-208-14.

Table 5-5. Equipment Level Operational Tests (Continued)

Item	Symptom	Cause	Remedy
9	Groups A and B matrix power supply number 1 has no +5-volt dc output. (From item 7, table 5-4.)	Defective power supply LM-CC-5. (See figure 5-11.)	Refer to Lambda Power Supply manual LM-CC-5 CM 32-6130-208-14.
10	Test oscillator power supply has no output. (From item 11, table 5-4.)	Defective power supply LM-CC-24. (See figure 5-6.)	Refer to Lambda Power Supply manual LM-CC-24 CM 32-6130-208-14.
11	Signal data converter power supply part number 3300-44037 has no output. (From item 24, table 5-4.)	Defective power supply PP6813/FLR-9(V) (See figure 5-3.)	Refer to figure 7-7. 1. Remove the signal data converter from rack 411. (Refer to paragraph 5-12, equipment removal.) 2. Remove the top cover and visually inspect the equipment. (See figure 5-3.) 3. Check fuse F1 at the rear of the equipment. 4. Connect a Simpson Model 260 Multimeter across the output of the power supply, and supply line voltage to the equipment. Power supply output is normally +5 volts dc ±0.5 volt dc. If no output is present, repair power supply per table 5-6.
12	A circuit function within the signal data converter does not operate.	Defective circuit	Troubleshoot the signal data converter per tables 5-6, 5-7, and 5-8.

5-11. Equipment Level Troubleshooting. (See table 5-6.)

Equipment items not covered by a referenced vendor manual are examined in the following tables and figures to localize a trouble to a replaceable unit (circuit card or component).

a. Signal Data Converter Troubleshooting. Examine test data carefully to determine what area of the converter is suspect and proceed according to instructions. The equipment must be removed from the rack for servicing (see paragraph 5-12.a).

1. Power Supply, Signal Data Converter. (Reference figures 5-3, 5-5, and 7-7.) Remove equipment covers and locate the power supply. Using figure 7-7 and table 5-6, locate the trouble and repair by replacing the defective component.

Table 5-6. Power Supply, Signal Data Converter, Troubleshooting

Item	Symptom	Cause	Remedy
1	No power supply output (Item 11, table 5-5).	Shorted output	Refer to figure 7-7. Remove short.
	Primary fuse is not blown.	Overvoltage tripped	Remove ac power from supply for 15 seconds to reset over-voltage circuit.
		Defective transistor Q1 to Q8	Replace defective transistor.
2	Same as item 1, except primary fuse is blown.	Supply overloaded	Remove overload.
		Shorted transistor Q8	Replace Q8.
		Defective transformer, diodes CR1-4, capacitor C1, C2, or C6	Replace defective component.
3	Power supply output has high ripple content.	Supply in overload condition	Remove overload.
		Defective capacitor C1, C2, C4, or C6	Replace defective capacitor.

2. Vector Voltmeter Control Word Circuit. This procedure tests the signal paths and decode circuits of the signal data converter. Set up the equipment as shown in figure 5-20. Apply primary power and allow equipment to warm up before proceeding to table 5-7. Refer to figure 5-4 for board locations and figure 7-6 for logic diagram. Refer to table 5-8, Board Location to Part Number Reference.

Table 5-7. Signal Data Converter Circuit, Troubleshooting

Step	Action	Result	Conclusion
		Vvm Control Word	
1	Set the differential simulator BIT I DISABLE switch to the DOWNJ position		
2	Set the APC TEST/NORMAL switch to the NORMAL position.		
3	Turn the simulator ON.		
4	Set the bit position switches as shown in steps 4.a. through 4.i. Position 0 is down and position 1 is up.		Remove the J2 connector from the signal data converter and measure +5 volts dc for each binary 1 shown on the J2 output pins in each step. Measure 0 volts dc for each binary 0.

	Bit Switch Positions									J2 Pin Numbers with Proper Decode															
	0	1	2	3	4	5	6	7	8	17	18	19	20	21	22	23	24	25	16	15	14	1	2	3	4	5
4a	1	0	0	1	1	1	1	0	0									1	1			1				
4b	0	0	0	1	0	1	0	1	0								1			1			1			
4c	1	1	1	0	1	0	1	1	0							1					1			1		
4d	0	1	1	0	0	0	0	0	1						1										1	
4e	1	0	1	0	0	0	1	0	1					1												1
4f	0	0	1	0	0	0	0	0	0				1													
4g	1	1	0	0	0	0	0	0	0			1														
4h	0	1	0	0	0	0	0	0	0		1															
4i	1	0	0	0	0	0	0	0	0	1																

			A faulty indicator at the J2 output indicates a fault in the decode represented by that bit. The faulty component is isolated by removing the signal data converter from the rack and signal tracing the faulty path until the specific component is identified.
5	Disconnect test equipment.	End of test.	
6	For counter circuits test, connect equipment as in figure 5-21.	Initial setup	Proceed to step 7.

Table 5-7. Signal Data Converter Circuit, Troubleshooting (Continued)

Step	Action	Result	Conclusion
	Set the equipment as follows: HP5245M Sample Rate to: Hold (use RESET button during frequency adjustment to update display.) Sensitivity to: 01 volt Function to: Frequency Time base to: HP606B Frequency to: 9999.999kHz Amplitude to: 1 millivolt Modulation to: CW	Initial control	
8	Connect test assembly to cable word 1.	Observe test assembly for following:(a "1" signifies lamp illuminated) BIT 0 1 2 3 | 4 5 6 7 | 8 91011 | 12131415 STATE 1 1 1 1 | 1 1 1 1 | 1 1 1 1 | 1 1 1 1 CODE D C B A / 4 2 2 1 | D C B A / 4 2 2 1 | D C B A / 4 2 2 1 | D C B A / 4 2 2 1 DIGIT 1 kHz | 100 Hz | 10 Hz | 1 Hz	Steps 8 through 15: When a fault is encountered, remove the cable connector from the put and ascertain if the fault is originating in the frequency counter or the signal data converter. If the frequency counter is at fault, repair in accordance with CM 32-6625-239-14.
9	Connect test assembly to cable word 2.	Observe for following: BIT 0 1 2 3 | 4 5 6 7 | 8 91011 | 12131415 STATE 1 1 1 1 | 1 1 1 1 | 1 1 1 1 | 1 1 1 1 CODE D C B A / 4 2 2 1 | D C B A / 4 2 2 1 | D C B A / 4 2 2 1 | D C B A / 4 2 2 1 DIGIT 10 MHz | 1 MHz | 100 kHz | 10 kHz	
10	Set HP606B frequency to 44444.444 kHz. Leave cable word 2 connected.	Observe for following: BIT 0 1 2 3 | 4 5 6 7 | 8 91011 | 12131415 STATE 0 1 1 0 | 0 1 1 0 | 0 1 1 0 | 0 1 1 0 DIGIT 10 MHz | 1 MHz | 100 kHz | 10 kHz	If the fault is in the signal data converter, refer to the logic diagram, figure 7-6, and replace the faulty card with a working spare. (Cards A3, A4, A5, or A6.)
11	Connect to cable word.	Observe for following: BIT 0 1 2 3 | 4 5 6 7 | 8 91011 | 12131415 STATE 0 1 1 0 | 0 1 1 0 | 0 1 1 0 | 0 1 1 0 DIGIT 1 kHz | 100 kHz | 10 Hz | 1 Hz	

Table 5-7. Signal Data Converter Circuits, Troubleshooting (Continued)

Step	Action	Result	Conclusion
12	Set HP 606B frequency to 22222.222 kHz. Leave cable word I connected.	Observe for following:	
13	Connect to cable word 2.	Observe for following;	
14	Set frequency of HP 606B to 22000.000 kHz. word 2 connected.	Observe for following: Leave cable	
15	Connect to cable word 1.	Observe for following:	
16	Disconnect test equipment.	End of test	Proceed to step 17.
17	To check the signal data converter attentuator, proceed as follows: Connect test equipment as in figure 5-22.	Initial setup	Proceed to step 18.
18	Set the equipment controls as follows: signal data converter - adjust attenuator to 0 dB. HP606B Frequency to: 18.0 MHz Amplitude to: +10 dBm on VVM. Modulation to: CW		Proceed to step 19.

BIT	0 1 2 3	4 5 6 7	8 91011	12131415
STATE	0 0 1 0	0 0 1 0	0 0 1 0	0 0 1 0
DIGIT	1 kHz	100 Hz	10 Hz	1 Hz

BIT	0 1 2 3	4 5 6 7	8 91011	12131415
STATE	0 0 1 0	0 0 1 0	0 0 1 0	0 0 1 0
Digit	10 MHz	1 MHz	100 kHz	10 kHz

BIT	0 1 2 3	4 5 6 7	8 91011	12131415
STATE	0 0 1 0	0 0 1 0	0 0 0 0	0 0 0 0
DIGIT	10 MHz	1 MHz	100 kHz	10 kHz

BIT	0 1 2 3	4 5 6 7	8 91011	12131415
STATE	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
DIGIT	1 kHz	100 Hz	10 Hz	1 Hz

Table 5-7. Signal Data Converter Circuits, Troubleshooting (Continued)

Step	Action	Result	Conclusion
	HP5245M SAMPLE RATE to: CW from OFF SENSITIVITY to: 0.IV FUNCTION to: Frequency TIME BASE to: 1 second HP8405A Channel to: A Amplitude Scale to: +10 dB		
19	Observe vm on vvm while adjusting attentuator in 1-dB steps. For each 1-dB attenuation added, the vvm should also change 1 dB in reading. Tolerance is +1 dB of attenuator scale calibration.	Correlation within tolerance Correlation out of tolerance	Attentuator okay. Replace attenuator. (not a maintenance item)
20	Disconnect test equipment	End of test	

Table 5-8. Board Location to Part Number Cross Reference, Signal Data Converter

Board Location	Part Number
(411A1) A1	3300-46027-1
A2	3300-44044-1
A3, A4, A5, and A6	3300-46028-1
A7	3300-44039-1
A8	3300-44040-1
A9	3300-44041-1
A10	3300-44042-1
A11	3300-44050-1
A12	3300-44049-1
Power Supply	3300-44037-1
Attenuator	3300-44063-1

b. Somc, Troubleshooting. Use the procedure in table 5-9 for V8 and table 5-10 for V7 to troubleshoot the somc. Figures 7-8 and 7-24 are used to determine which boards are to be replaced. Figure 5-16 is used to determine board location. Replaceable parts in the controller-control panel area involved are boards, lamps, and lamp/ control fixtures. An aid to troubleshooting the somc is the theory of operation in section IV of the manual. Figures 5-9 and 7-16 (alarm junction box) should be considered as an aid to troubleshooting roundhouse alarm inputs. Figures 7-14 and 7-15 also are useful for checking airflow alarm routing. Rear view of the somc is shown in figure 5-15.

Table 5-9. Somc, Troubleshooting (V8)

Step	Action	Result	Conclusion
1	Apply power to somc, silence alarm, perform lamp test.	All lamps are ililum-inated.	Replace any lamp that fails to illuminate. NOTE: If flasher is in-operative, replace board A101 or A102.
2	Use single-ended signal simulator test fixture. Place power ON-OFF switch to OFF position. Place bit switches 0 through 15 on test fixture to the ON (up) position. Connect test cable 3300-68035-1 between test fixture and J1 on rack 217. The two access panels above the somc must be removed for this test.		Proceed to step 3.
3	Set bit switch 0 of test fixture to OFF (down) position. Press SILENCE ALARM. Press RH401 switch. Reset bit switch 0 of test fixture to ON (up)	RH401 flashes red ON and OFF. Audible alarm sounds. Audible alarm is si-lenced. RH401 is il-luminated steady red. RH401 lamp is ex-tinguished.	If inoperative, replace boards A201, A103, A104, A107, or lamp fixture. (See figure 7-8, sheet 1.)
4	Repeat step 3 procedure for each of the following BIT SWITCH INDICATOR 1 RH403 2 RH404 3 RH408 4 RH415	 Flashing Flashing Flashing Flashing	If inoperative, see figure 7-8, sheet 1 for board replacement deter-mination

Table 5-9. Somc, Troubleshooting (V8) (Continued)

Step	Action	Result	Conclusion
	5 RH416 6 RH420 7 RH421	Flashing Flashing Flashing	
5	Set bit switch 8 of test fixture to down position.	RH 414 5V flashes red ON and OFF. OLM&T ERROR is illuminated steady yellow. Audible alarm will sound.	If inoperative, see figure 7-8, sheet 2 for board replacement determination.
	Press RH 414 5V. Reset bit switch to up position.	RH 414 5V is illuminated steady red. Indicator is extinguished.	
6	Repeat step 5 for bit switch 9.	RH 414 8V is activated.	If inoperative, use figure 7-8, sheet 2 for board replacement determination.
7	Remove test fixture test cable from Ji and the test fixture. Connect 32-pin test cable assembly between test fixture and J2.		
8	Repeat step 5 for each of the following BIT SWITCH INDICATOR O OPS 203 5V 1 OPS 203 8V 2 OPS 203 24V OLM&T ERROR lamp is ilium-inated with setting of bits 0, 1, and 2 to down position and extinguished with resetting of bits to up position.	 Flashing Flashing Flashing	If inoperative, see figure 7-8, sheet 2 for board replacement determination.
9	Remove test cable from J2 and insert into J3 of rack 217. Repeat step 3 for each of the following		If inoperative, see figure 7-8, sheet 3 for board replacement determination.

Table 5-9. Somc, Troubleshooting (V8) (Continued

Step	Action	Result	Conclusion
	BIT SWITCH INDICATOR 3 OPS 203 5V 4 OPS 203 8V 5 OPS 203 24V	 Flashing Flashing Flashing	
10	Remove test cable from J3 on rack 217 and from test fixture. Connect 55 pin test cable between J5 of rack 217 and differential simulator test fixture. Ensure that bit switches of test fixture are in the down position. Turn the power switch to ON.		
11	Set bit switch 0 on test fixture to up position. Set bit switch 0 of test fixture to down position.	ASR RUN, A OPS 218 A is illuminated steady green. ASR RUN, A OPS 218 A is extinguished.	If inoperative, see figure 7-8 for board replacement determination.
12	Repeat procedure of step 16 for each of the following. Where lamps are flashing, press the flashing indicators and they are illuminated steadily. BIT SWITCH INDICATOR 1 ASR FAULT OPS 218 A 2 ASR RUN OPS 216 B 3 ASR FAULT OPS 216 B 4 CPU PWR FAIL OPS 210 A 5 CPU PWR FAIL OPS 211 B 6 WDT OPS 210 A 7 WDT OPS 211 B 8 CPU FAULT OPS 210 A	 Steady Green Steady Green Steady Green Flashing Flashing Flashing Flashing Flashing	If inoperative, see figure 7-8 for board replacement determination.

Table 5-9. Somc, Troubleshooting (v8) (Continued)

Step	Action	Result	Conclusion or Remedy
	9 CPU FAULT OPS 211 B	Flashing	
	10 Computer Status	OFF LINE A Illuminated	
	11 Computer Status	OFF LINE B Illuminated	
	12 Computer Status	STBY-A Illuminated	
	13 Computer Status	STBY-B Illuminated	
	14 Computer Status	PRIM-A Illuminated	
	15 Computer Status	PRIM-B Illuminated	
13	Remove test cable from J5 of rack 217 and connect to J6 of rack 217. Verify all switches of test assembly are in the down position.	Days display 000.	Proceed to step 14.
14	Set the following bit switches to up position to obtain readouts under the DAYS designation. indicator unit, see figure 5-19 and paragraph		If inoperative, see figure 7-8, sheet 4 for board replacement determinatlon. For repair of indicator unit, see figure 5-19 and paragraph 5-12.b.2.d.

Hundreds		Tens		Units	
Bits	Display	Bits	Display	Bits	Display
None	0	None	0	None	0
3	1	7	1	11	1
2	2	6	2	10	2
2 & 3	3	6 & 7	3	10 & 11	3
		5	4	9	4
		5 & 7	5	9 & 11	5
		5 & 6	6	9 & 10	6
		5,6,& 7	7	9, 10 &11	7
8	8				
		4 & 7	9	8& 11	

15	Set the following bit switches to up position.		If inoperative, see figure 7-8, sheet 5 for board replacement determination.

Table 5-9. Somc, Troubleshooting (V8) (Continued)

Step	Action	Result	Conclusion or Remedy
	BIT SWITCH 12 MAG TAPE RUN OPS 212 I-T illuminated 13 MAG TAPE FAULT OPS 212 I-T illuminated 14 MAG TAPE RUN OPS 212 2-B illuminated 15 MAG TAPE FAULT OPS 212 2-8 illuminated Reset bit switches to down position.	INDICATOR	
16	Remove test cable from test fixture and from J6 of rack 217. cable to 16 differential line receiver test fixture.	Tty inputs ILLEGAL SOMC FORMAT Connect test	Proceed to step 17
17	Connect test cable to J7 of rack 217. Turn POWER switch on 16 line receiver to ON. Press BEAMFORM switch.	BEAMFORM lamp is illuminated white and bit 5 is indicated on test fixture.	If inoperative, see figure 7-8, sheet 5 for board Replacement determination.
	Press BEAMFORM switch. extinguished and bit 5 is extinguished.	BEAMFORM lamp is	
18	Press ANT TEST switch	ANT TEST switch is illuminated white and bit 6 is indicated.	Same as step 17.
	Press ANT TEST switch.	ANT TEST switch lamp is extinguished and bit 6 is extinguished.	
19	Press RFSM-X-PT switch.	RFSM-X-PT lamp is illuminated white and bit 7 is indicated	Same as step 17.

Table 5-9. Somc, Troubleshooting (V8) (Continued)

Step	Action	Result	Conclusion or Remedy
	Press RFSM-X-PT switch.	RFSM-X-PT lamp is extinguished and bit 7 is extinguished.	
20	Press OSC TEST switch	OSC TEST lamp is illuminated white and bit 8 is indicated.	Same as step 17.
	Press OSC TEST switch.	OSC TEST lamp is extinguished and bit 8 is extinguished.	
21	Press OLM&T FAULT switch.	OLM&T switch lamp is illuminated white and bit 9 is indicated.	Same as step 17.
	Press OLM&T FAULT switch.	OLM&T switch lamp is extinguished and bit 9 is extinguished.	
22	Press CPU CHANGEOVER INHIBIT switch,	CPU CHANGEOVER lamp is illuminated white and bit 10 is indicated on the test fixture.	Same as step 17.
	Press CPU CHANGEOVER INHIBIT switch.	CPU CHANGEOVER lamp is extinguished and bit 10 is extinguished.	
23	Press CPU OFF-LINE A OPS 210 switch.	CPU OFF-LINE, A OPS 210 lamp is illuminated white and bit 11 is indicated.	Same as step 17.
	Press CPU OFF-LINE A OPS 210 switch.	CPU OFF-LINE A OPS 210 lamp is extinguished and bit 11 is extinguished.	

Table 5-9. Somc, Troubleshooting (V8) (Continued)

Step	Action	Result	Conclusion or Remedy
24	Press CPU OFF-LINE B OPS 211 switch. Press CPU OFF-LINE B OPS 211 switch.	CPU OFF-LINE B OPS 211 lamp is illuminated white and bit 12 is indicated. CPU OFF-LINE B OPS 211 lamp is extinguished and bit 12 is extinguished.	Same as step 17.
25	This test verifies the operation of the CPU PRIMARY SELECT A & B. Press the CPU primary select switch to cause the "A" lamp to illuminate if not already in this condition.	The "A" lamp is illuminated white and bit 13 is indicated on the test fixture.	If inoperative, see figure ure 7-8, sheet 7 for board replacement determination.
26	Press the CPU PRIMARY SELECT switch.	CPU PRIMARY SELECT indicator is illuminated "B" white and bit 14 is indicated on the test fixture.	Same as step 25.
27	Press OLM&T PRINT switch. Press OLM&T PRINT switch.	OLM&T PRINT switch is illuminated white and bit 15 is indicated on the test fixture. OLM&T PRINT lamp is extinguished and bit 15 is extinguished.	Same as step 25.
28	Remove test cable from J7 of rack 217 and test fixture.	Proceed to step 29.	

Table 5-9. Somc, Troubleshooting (V8) (Continued)

Step	Action	Result	Conclusion or Remedy
	Connect the same test cable between 16 line single-ended simulator test fixture and J8 of rack 217 after determining that the POWER switch on the test fixture is OFF. Set all bit switches of the test fixture to the up position.	NOTE: POWER switch on single-ended signal simulator is OFF for this test.	
29	Set bit switches 0 through 14, respectively, to the down position and the indicated RFSM TEMP lamps are illuminated. 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 Reset the bit switches to up position.	 1A1 illuminated 1A2 illuminated 1A3 illuminated 2A1 illuminated 2A2 illuminated 2A3 illuminated 2A4 illuminated 3A1 illuminated 3A2 illuminated 3A3 illuminated 3A4 illuminated 4AI illuminated 4A2 illuminated 4A3 illuminated 4A4 illuminated The lamps are extinguished.	Same as step 25.

Table 5-9. Somc, Troubleshooting (V8) (Continued)

Step	Action	Result	Conclusion or Remedy
30	Remove the test cable from J8 of rack 217 and insert into J9 of rack 217.	Proceed to step 31.	
31	Repeat step 27 procedure.		Same as step 25.
	0	5A1 illuminated	
	1	5A2 illuminated	
	2	5A3 illuminated	
	3	5A4 illuminated	
	4	6A1 illuminated	
	5	6A2 illuminated	
	6	6A3 illuminated	
	7	6A4 illuminated	
	8	6A5 illuminated	
	9	7A1 illuminated	
	10	7A2 illuminated	
	11	7A3 illuminated	
	12	7A4 illuminated	
	13	7A5 illuminated	
32	Remove the test cable from J9 of rack 217 and insert into J1O.		Proceed to step 33.
33	Repeat step 27 procedure.		Same as step 25.
	0	8A1 illuminated	
	1	8A2 illuminated	
	2	8A3 illuminated	
	3	8A4 illuminated	
	4	8A5 illuminated	
	5	9A1 illuminated	
	6	9A2 illuminated	
	7	9A3 illuminated	
	8	9A4 illuminated	
	9	9A5 illuminated	

Table 5-9, Somc, Troubleshooting (V8) (Continued)

Step	Action	Result	Conclusion or Remedy
34	Remove the test cable from JO1 of rack 217 and insert into J11 of rack 217.		Proceed to step 35
35	Repeat step 28 procedure for the following RFSM PWR SPLY FAIL lamps, respectively.		
	0	N1A1 illuminated	
	1	N2A1 illuminated	
	2	N4A1 illuminated	
	3	N5A1 illuminated	
	4	NIA2 illuminated	
	5	N2A2 illuminated	
	6	N4A2 illuminated	
	7	N5A2 illuminated	
	8	N6A1 illuminated	
	9	N6A2 illuminated	
	11	RFSM PWR SUPPLY AIR FLOW illuminated	
36	Remove the test cable from J11 of rack 217 and set POWER switch to OFF.		Test finished.

Table 5-10. Somc, Troubleshooting (V7)

Step	Action	Result	Conclusion or Remedy
1	Apply power to somc, silence alarm, perform lamp test.	All lamps are illuminated.	Replace any lamp that fails to illuminate . If flasher is inoperative, replace board A101O or A102.
2	Use single-ended signal simulator test fixture. Place power ON/OFF switch to OFF position. Place bit switches O through 15 on test fixture to the ON	Proceed to step	

Table 5-10. Somc, Troubleshooting (V7)

Step	Action	Result	Conclusion or Remedy
	(up) position. test cable between test fixture and J1 of rack 217 (somc). The two access panels must be removed for this test.	Connect a	
3	Set bit switch 0 of test fixture to OFF (down) position.	RH401 flashes red ON and OFF, audible alarm sounds.	If inoperative, replace boards A201, A103, A104, A107, or lamp fixture. See figure 7-24.
	Press SILENCE ALARM.	Alarm silences.	
	Press RH401 switch	RH401 is illuminated steady red.	
	Reset bit switch 0 to up position.	RH401 is extinguished,	
4	Repeat step 3 procedure for each of the following	If inoperative, see figure 7-24, sheet I for	board replacement determination.
	BIT SWITCH / INDICATOR		
	1 RH403	Flashing	
	2 RH404	Flashing	
	3 RH408	Flashing	
	4 RH415	Flashing	
	5 RH416	Flashing	
	6 RH420	Flashing	
	7 RH421	Flashing	
5	Set bit switch 8 of test fixture to down position.	RH414 5V flashes red ON and OFF. OLMT ERROR is illuminated steady yellow. Audible alarm sounds.	If inoperative, see figure 7-24, sheet 2 for board replacement determination.
	Press RH414-5Vo	RH414 5V is illuminated steady red.	
	Reset bit switch 8 to up position.	Indicator is extinguished.	

Table 5-10. Somc, Troubleshooting (V7 (Continued)

Step	Action	Result	Conclusion or Remedy
6	Repeat step 5 for bit switch 9.	RH414 8V is activated.	Same as step 5.
7	Remove test fixture test cable from J1 and the test fixture. Connect cable assembly 32-pin test between test fixture and J2.		Same as step 5.
8	Repeat step 5 for each of the following BIT SWITCH INDICATOR 0 OPS203 5V 1 OPS203 8V 2 OPS203 24V OLM&T ERROR lamp is illuminated with setting of bits 0, 1, and 2 to down position and extinguished with resetting of bits to up position. test equipment.	Same as step 5. Flashing Flashing Flashing Disconnect	
9	Remove test cable from J2 of rack 217 and from test fixture. test cable between J5 of rack 217 and differential simulator test fixture. Ensure that bit switches of test fixture are in the down position. the power switch to ON.	Connect 55-pin Turn	
10	Set bit switch 0 to up position. Set bit switch 0 to down position.	ASR-RUN A OPS218-A is illuminated a steady green. ASR-RUN A OPS218-A is extinguished.	If inoperative, see figure 7-24 for board replacement determination.

Table 5-10. Somc, Troubleshooting (V7) (Continued)

Step	Action	Result	Conclusion or Remedy
11	Repeat procedure of step 10 for each of the following. Where lamps are flashing, press the indicators to illuminate steadily. BIT SWITCH — INDICATOR 1 — ASR FAULT OPS218 A 2 — ASR RUN OPS216 B 3 — ASR FAULT OPFS21(B 4 — CPU PWR FAIL UPS210 A 5 — CPU PWR FAIL OPS211 U 6 — WDT OPS210 A 7 — WDT OPS211 B 8 — CPU FAULT OPS210 A 9 — CPU FAULT OPS211 8 10 — Computer Status 11 — Computer Status 12 — Computer Status 13 — Computer Status 14 — Computer Status 15 — Computer Status	Steady green Steady green Steady green Flashing Flashing Flashing Flashing Flashing Flashing OFF-LINE A Illuminated OFF-LINE B Illuminated STBY A Illuminated STBY B illuminated PRIM A Illuminated PRIM B Illuminated	If inoperative, see figure 7-24 for hoard replacement determination.
12	Remove test cable from J5 of rack 217 and connect to J6 of rack 217, Verify all switches of test assembly are in the down position.	Days display reads 000,	Proceed to step 13.

Table 5-10. Somc, Troubleshooting (V7) (Continued)

<table>
<tr><th>Step</th><th colspan="4">Action</th><th colspan="2">Result</th><th>Conclusion or Remedy</th></tr>
<tr><td>13</td><td colspan="4">Set the following bit switches to up position to obtain the readouts under the Days designation</td><td colspan="2"></td><td rowspan="3">If inoperative, see figure 7-24, sheet 4 for board replacement determination
For repair of indicator unit, see figure 5-19 and paragraph 5-12.b.2.d,</td></tr>
<tr><td colspan="2">Hundreds</td><td colspan="2">Tens</td><td colspan="2">Units</td></tr>
<tr><td>Bits</td><td>Display</td><td>Bits</td><td>Display</td><td>Bits</td><td>Display</td></tr>
<tr><td>None
3
2
2 & 3</td><td>0
1
2
3</td><td>None
7
6
6 & 7
5
5 & 7
5 & 6
5,6 &7
4
4 & 7</td><td>0
1
2
3
4
5
6
7
8
9</td><td>None
11
10
10 & 11
9
9 & 11
9 & 10
9,10& 11
8
8 & 11</td><td>0
1
2
3
4
5
6
7
8
9</td><td></td></tr>
<tr><td>14</td><td colspan="4">Set the following bit switches to up position.

Bit 12

Bit 13

Bit 14

Bit 15

Reset bit switches.</td><td colspan="2">

MAG TAPE RUN OPS212 1-T is illuminated.

MAG TAPE FAULT OPS212 I-T is illuminated.

MAG TAPE RUN OPS212 2-T is illuminated.

MAG TAPE FAULT OPS212 2-B is illuminated.</td><td>If inoperative, see figure 7-24, sheet 5 for board replacement determination.</td></tr>
</table>

Table 5-10. Somc, Troubleshooting (V7) (Continued)

Step	Action	Result	Conclusion or Remedy
15	Remove test cable from test fixture and from J6 of rack 217. Connect test cable to 16 differential line receiver test fixture.		Proceed to step 16.
16	Connect test cable to J7 of rack 217.		
	Press BEAMFORM switch.	BEAMFORM lamp is illuminated white and bit 5 is indicated on test fixture.	If inoperative, see figure 7-24 sheet 5 for board replacement determination.
	Press BEAMFORM switch.	BEAMFORM lamp is extinquished and bit 5 is extinguished.	
17	Press ANT TEST switch.	ANT TEST switch is illuminated white and bit 6 is indicated.	Same as step 16.
	Press ANT TEST switch.	ANT TEST switch lamp is extinguished and bit 6 is extinguished.	
18	Press RFSM X-PT switch.	RFSM X-PT lamp is illuminated white and bit 7 is indicated.	Same as step 16.
	Press RFSM X-PT switch.	RFSM-X-PT lamp is extinguished and bit 7 is extinguished.	
19	Press OSC. TEST switch.	OSC. TEST lamp is illuminated white and bit 8 is indicated.	
	Press OSC. TEST switch.	OSC. TEST lamp is extinguished and bit 8 is extinguished.	

Table 5-10. Somc, Troubleshooting (V7) (Continued)

Step	Action	Result	Conclusion or Remedy
20	Press OLM&T FAULT switch.	OLM&T FAULT switch lamp is illuminated white and bit 9 is indicated.	Same as step 16.
	Press OLM&T FAULT	OLM&T FAULT switch lamp is extinguished and bit 9 is extinguished.	
21	Press CPU CHANGEOVER INHIBIT switch.	CPU CHANGEOVER lamp is illuminated white and bit 10 is indicated on the test fixture.	Same as step 16.
	Press CPU CHANGEOVER INHIBIT switch.	CPU CHANGEOVER lamp is extinguished and bit 10 is extinguished.	
22	Press CPU OFF-LINE A OPS210 switch.	CPU OFF-LINE A OPS210 lamp is illuminated white and bit 11 is indicated.	Same as step 16.
	Press CPU OFF-LINE A OPS210 switch.	CPU OFF-LINE A OPS210 lamp is extinguished and bit 11 is extinguished.	
23	Press CPU OFF-LINE B OPS211 switch.	CPU OFF-LINE B OPS211 lamp is illuminated white and bit 12 is indicated.	Same as step 16.
	Press CPU OFF-LINE B OPS211 switch.	CPU OFF-LINE B OPS211 lamp is extinguished and bit 12 is extinguished.	
24	This test verifies the operation of the CPU PRIMARY SELECT A & B.	The "A" lamp is illuminated white and bit 13 is indicated on the test fixture.	If inoperative, see figure 7-24, sheet 7 for board replacement determination.

Table 5-10. Somc, Troubleshooting (V7) (Continued)

Step	Action	Result	Conclusion or Remedy
	Press the CPU primary select switch to cause the "A" lamp to be illuminated if not already in this condition.		
25	Press the CPU PRIMARY SELECT switch.	CPU PRIMARY SELECT indicator is illuminated "B" white and bit 14 is indicated on the test fixture.	Same as step 24.
26	Press the OLM/T PRINT switch.	OLM/T PRINT switch is illuminated white and bit 15 is indicated on the test fixture.	Same as step 24.
	Press OLM/T PRINT switch.	OLM/T PRINT lamp is extinguished and bit 15 is extinguished.	
27	Remove test cable from J7 of rack 217 and test fixture.		Proceed to step 28.
	Connect the same test cable between the single-ended simulator test fixture and J8 of rack 217 after determining that the POWER switch on the test fixture is OFF.		
	Set all bit switches of the test fixture to the ON position.		
28	Set bit switches 00 through 15, respectively, to down position and the indicated RFSM TEMP lamps re illuminated.		Same as step 24.

Table 5-10. Somc, Troubleshooting (V7) (Continued)

Step	Action	Result	Conclusion or Remedy
	00	1A1 is illuminated	
	01	1A2 is illuminated	
	02	1A3 is illuminated	
	03	2A1 Is illuminated	
	04	2A2 is illuminated	
	05	3AI is illuminated	
	06	3A2 is Illuminated	
	07	4A1 is illuminated	
	08	4A2 is illuminated	
	09	5A1 is illuminated	
	10	5A2 is illuminated	
	11	6A1 is illuminated	
	12	6A2 is illuminated	
	Reset the bit switches to up position.	The lamps are extinguished.	
29	Remove the test cable from J8 of rack 217 and insert into J9 of rack 217.		Proceed to step 30.
30	Repeat step 28 procedure.		
	0	7A1 Is illuminated	
	1	7A2 is illuminated	
	2	7A3 is illuminated	
	3	8A1 is illuminated	
	4	8A2 is illuminated	
	5	9A1 is illuminated	
	6	9A2 is illuminated	
	7	9A3 is illuminated	
31	Repeat step 27 procedure for the following RFSM PWR SPLY FAIL lamps, respectively.		
	0	N1A1 Is illuminated	
	1	N2A1 is illuminated	
	2	N4A1 is illuminated	
	3	N5A1 is illuminated	

Table 5-10. Somc, Troubleshooting (V7) (Continued)

Step	Action	Result	Conclusion or Remedy
	4 5 6 7 11	N1A2 illuminated N2A2 illuminated N4A2 illuminated N5A2 illuminated RFSM PWR SUPPLY AIR FLOW illuminated	
32	Remove the test cable from J11 of rack 217 and power switch to OFF.		Test finished.

c. Test Oscillator Troubleshooting. The OSC TEST pushbutton on the somc is used to initiate a test of the frequency of each of the 18 reference oscillators. In this test, the output of each oscillator is routed from the A group matrix to the B group matrix, to the frequency counter. The frequency counter output is then routed, via the signal data converter and cable scanner multiplexer, to the computer for verification of accuracy. With the PRINT button on the somc pressed, a complete oscillator test cycle results in a tty printout as follows:

OLMT OSC TEST START (signifies start of test)

XXX YY YY YY Z (denotes day of year and hours, minutes and seconds, GMT)

OSC XX FREQ YYYYYYYY (appears 18 times, one for each oscillator and identifies oscillator number and frequency)

If an oscillator frequency is detected which is out of the tolerance limits, an additional fault message is printed, as follows:

OSC XX FREQ FAULT (identifies number of faulty oscillator)

REF YYYYYYYY TOL YY FREQ YYYYYYYY (Y represents frequency)

In addition, a special test may be requested from the tty by typing the message:

TEST OSC FREQ XX

Where:

XX identifies the oscillator number, 1-18

The system response is the same message as appears during a regular test with the print button pressed.

In the event a single oscillator fails the frequency test, it is relatively safe to assume that the fault is in the oscillator since the frequency counter, signal data converter, and cable scanner multiplexer circuits used, are the same for all oscillators. In the event a similar failure indication is present for all oscillators, the problem is in the common circuitry of one of these three units. The frequency counter output word troubleshooting procedure associated with the signal data converter circuits, as outlined in table 5-7 should be used to isolate the source of the problem. If the oscillator is determined to be at fault, the oscillator frequency check procedure in section 6 should be followed. If the failure prevents adjustment to the proper stable output, the oscillator must be replaced.

5-12. Repairs Procedures.

a. Equipment Removal and Replacement. All monitor and test group equipments are secured to rack mounting surfaces with retaining screws accessible from either the front or rear of the racks. In general, an equipment is prepared for removal by disconnecting all cables to the equipment and removing the retaining screws. The equipment is then removed by withdrawing toward the person removing the retaining screws.

CAUTION

The following precautions must be observed for personnel safety and equipment protection during removal or replacement.

1. In all cases, input power is to be removed from the equipment before disassembly.
2. Power supply number 1, in rack 411, and power supply number 2 (V7) or number 3 (V8), in rack 203, require two people for removal because of the weight of the equipment.
3. When removing the digital interface unit (diu) of any olm&t matrix from its case, care must be taken that exposed pins at the bottom of the equipment are not damaged during withdrawal across the mounting flange.

b. Module or Card Removal and Replacement. In all cases, power must be removed from the equipment being repaired to prevent damage to circuit components and to prevent electrical shock to personnel.

1. Plug-in Module/Card Removal and Replacement. Remove all connections or restraining devices to the item being removed. Withdraw the item with a gentle pulling and rocking motion until the connector releases the item and carefully withdraw the module/card until it is clear of other components. Reverse the procedure to replace the item.

2. Hard-Wired Module Removal and Replacement. Carefully note all electrical connections to the module being replaced for future reference. Remove electrical connections. Remove mounting screws and retaining hardware. Carefully withdraw the module from the equipment until clear. Reverse the procedure for replacement.

c. Component Removal and Replacement. Component assemblies such as attenuators, lamp assemblies, or test oscillators (see figure 5-6) are removed and replaced as in

paragraph 5-12.b.2. Soldered components are removed and replaced according to best soldering practices by qualified technicians.

d. Fiber Optic Display Repair. (See figure 5-19.)

1. To replace lamps in the fiber optic display assembly, perform the following:

(a) Prior to removing the fiber optic display from the unit, remove the lamp assembly by pulling outward on the flanged area.

(b) Remove the two contact block retaining screws and remove the block.

(c) Replace defective lamps and replace the contact block. Tighten screws to pull contact block against lamp assembly.

2. To replace the lamp driver chip, perform the following steps:

(a) Set POWER switch to OFF.

(b) Carefully mark the wires connected to the fiber optic display jack to facilitate reassembly and remove the wires.

(c) Remove the panel fiber optic display assembly from the unit panel by grasping the fiber optic unit at the rear of the assembly and working the unit out through the front panel.

(d) Bend up the maintenance release retaining clips (4 each).

(e) Pull the driver housing from the unit.

(f) Using a solder sucker and soldering iron, remove solder from each lamp driver chip connector.

(g) Remove the chip.

(h) Replace the chip and resolder each connection.

(i) Observing guide pin number 5, replace the driver housing.

(j) Bend down the retaining clips.

(k) Insert the fiber optic unit in the front panel by firmly seating the unit from the front.

(l) Carefully replace the wires in the fiber optic display jacks.

e. Vector Voltmeter Replacement. Each time the vvm is replaced or repaired, the phase amplitude and frequency adjustments described in paragraph 5-13.e. must be performed with emphasis on the phase offset adjustment described in the procedure.

5-13. Alignment and Adjustment.

a. Power Supply Number 1, PP-6811/FLR-9(V) Test. (See figures 5-11, 5-14, 7-3, and 7-11.) This test is performed to determine that proper working voltages are supplied to the group A and B switch matrices.

1. Test Equipment Required. Fluke Model 853A differential voltmeter or an electronic multimeter having required accuracy.

2. Procedure. Perform the following steps:

NOTE

OLM&T FAULT must be set before performing this test.

Step 1. To check the 8-volt power supply output, turn the power switch at the rear of the rack 414A3 to OFF. Remove the supply cable at J2.

Step 2. Turn the power supply switch to ON and set the voltmeter range switch to 50 volts dc. Attach the test leads to read the voltage between pin D of the cable and chassis ground. Adjust the voltmeter controls to measure the voltage.

Step 3. This voltage should measure 8 volts +0.25 volts. If the voltage reading does not fall within these limits, adjust the power supply output. Figure 5-11 shows the point of adjustment. Figure 7-3 shows the dc power distribution from this supply.

Step 4. To check the 5-volt power supply output, connect the multimeter leads to measure between pin G on the cable connector and chassis ground. Turn the power switch to ON. Adjust the voltmeter controls to produce a differential null.

Step 5. The voltage should read 5 volts ±0.25 volt. If the reading does not fall within these limits, adjust the power supply output. Figure 5-11 shows the point of adjustment.

Step 6. Turn the power switch to OFF and reconnect the power cable to the diu at J2. This concludes the power supply number I test.

b. Power Supply Check, PP-6810/FLR-9(V) (Number 2) (V7) and PP-6814/FLR-9(V) (Number 3) (V8) Test, Matrix C. (See figures 5-12, 5-13, 5-10, 7-12 and 7-13.

1. Test Equipment Required: John Fluke Model 853A differential voltmeter (an electronic multimeter having the required accuracy can be used for this test).

2. Procedure:

NOTE

OLM&T FAULT must be set before performing this test.

Step 1. To check the 5-volt power supply source, (203A13 for V8 and 204A12 for V7), turn the power switch at the rear of the power supply to OFF and remove the supply cable at J2.

Step 2. Set the John Fluke 853A Voltmeter to the 50-volt dc range and connect it from pin G of the cable to pin H (see figure 7-12).

Step 3. Turn the power switch to ON. Adjust the voltmeter controls to produce a differential null. The voltage should measure 5 volts ±0.25 volts. If the voltage reading does not fall within these limits, adjust the power supply. See figure 5-10 or 5-13 for the point of adjustment.

Step 4. Measure the 8-volt supply from pin D to pin E.

Step 5. The voltage should measure 8 volts ±-0.25 volt. If the voltage reading does not fall within these limits, adjust the power supply (see figures 5-10 or 5-13 for the point of adjustment).

Step 6. Measure the 24-volt supply from pin A to pin B.

Step 7. The 24-volt supply output should measure 24 volts ±0.25 volt. If not, adjust the power supply. Refer to figure 5-10 or 5-13 for the point of adjustment.

c. Power Supply Check PP-6809/FLR-9(V), Somc. (See figures 5-16, 5-18, and 7-2.)

1. Test Equipment Required: John Fluke Model 853A differential voltmeter (an electronic multimeter having the required accuracy can be used for this test).

2. Procedure:

Step 1. Set the power switch to ON for rack 217 and apply power to the test equipment.

Step 2. Open the rear door or rack 217 to gain access to the controller.

Step 3. Referring to figure 5-16, connect the voltmeter to differentially read -7 volts dc at A224-29 or -59 with respect to A224-15 or 45.

Step 4. This voltage should read -7 volts dc ±0.25 volt dc. If necessary, adjust the power supply output. Refer to figure 5-18 for the point of adjustment.

d. Power Supply Check, 3300-46119. Somc Dual. Set up procedure and test equipment for this check is the same as paragraph c. Refer to figures 5-16, 5-17, and
7-2. Perform the following steps.

Step 1. Set the power switch for rack 217 to ON and apply power to the test equipment.

Step 2. Open the rear door of rack 217 to gain access to the controller.

Step 3. Measure +5 volts dc ±0.25 volt dc on pins 30 or 60 of AO11 with respect to pins 15 or 45 of AlO1.

Step 4. Measure +25 volts dc ±0.5 volt dc on pins 29 or 59 of A117 with respect to pins 15 or 45 of A117.

Step 5. Should either power supply need adjustment, refer to figure 5-17 for the point of adjustment.

e. Phase and Amplitude Adjustments (V8) (V7). (See figures 1-2, 1-3, and 1-4 and table 5-11, 5-12 and 5-13.) These tests are performed to calibrate the monitor and test equipment and to verify proner operation throughout the frequency range. The tests are performed using simulated computer input words to the olm&t A matrix while using the vvm and counter in the manual mode to verify proper equipment operation.

Step 1. Set the B matrix to a test cable configuration by setting the BEAMFORM and PRINT controls on the somc control panel and observing the tty printout. When the tty has printed out first test cable results, set the OLM&T FAULT control.

CAUTION

The somc operator is not to attempt any olm&t functions during this calibration procedure.

Step 2. Connect the Simulator, Differential Signal SM664/FLR-9(V) (differential simulator) to 414A1A5Jl. (See figure 1-2.)

Step 3. Disconnect the vector voltmeter (vvm) control cable at 411A2JO11. (See figure 1-2.)

NOTE

The simulator setup words given are formatted to correspond with the simulator bit switch arrangement. Bits 0 through 15 are counted from left to right. Strobe bit 0 is disabled in the DIU.

Step 4. Set the vvm MODE switch to CHANNEL B and set the PHASE OFFSET switch to zero degrees.

Step 5. Set the differential simulator bit switches to 0100 0001 0100 1000.

Step 6. Set the FREQ RANGE switch on vvm to position where APC UNLOCK lamp is out.

Step 7. Set the signal source assembly ATTENUATOR LEVEL SET control on the SIGNAL SOURCE ASSY/OLM&T (see figure 1-2 and figure 3-3) for the 1.5-MHz oscillator to the amplitude shown in table 5-11 for V8 or table 5-12 for V7.

Table 5-11. Test Cable Verification Values (V8)

OSC Number	Frequency in MHz	Phase in Degrees (t5°)	Amplitude in Millivolts
1	1.5	-2.85	370
2	2.0	-3.35	360
3	3.0	-3.80	355
4	3.5	-4.35	355
5	4.5	-5.60	365
6	6.0	-7.60	368
7	6.0	-14.5	378
8	7.5	-18.0	438
9	9.0	-21.0	390
10	12.0	-27.0	462
11	14.0	-31.9	462
12	18.0	-40.0	505
13	18.0	+58.5	491
14	19.O	+62.0	462
15	22.0	+72.0	474
16	24.0	+78.0	490
17	27.0	+88.0	495
18	30.0	+98.0	649

Table 5-12. Test Cable Verification Values (V7)

OSC Number	Frequency in MHz	Phase in Degrees (±5°)	Amplitude in Millivolts
1	1.5	-2.8	378
2	2.0	-3.4	335
3	3.0	-4.7	353
4	3.5	-5.2	345
5	4.5	-7.0	350
6	6.0	-9.1	375
7	6.0	-16.1	363
8	7.5	-20.2	438
9	9.0	-23.7	438
10	12.0	-31.4	420
11	14.0	-37.1	489
12	18.0	-46.8	533
13	18.0	+62.3	488
14	19.0	+65.9	490
15	22.00	+75.9	469
16	24.0	+84.2	535
17	27.0	+94.4	530
18	30.0	+103.4	648

Table 5-13. Oscillator Test Setup Words (V8)(V7)

Oscillator Frequency (MHz)	Rack 414 Word* -	
1.5	0100/0001/0100/1000	
2.0	0100/00oO/O00/1000	
3.0	0100/0011/0100/1000	BAND A
3.5	OlO0 /0100/O100/1000	
4.5	0100/0101/0100/1000	
6.0	oo00/ollo/oloo/l0oo	
6.0	O010/0001/l001/0110	
7.5	0010/0010/1001/0110	
9.0	0010/0011/1001/0110	BAND B
12.0	0010/0100/1001/0110	
14.0	0010/0101/1001/0110	
18.0	0010/0110/1001/0110	
18.0	000 1/001/0100/1000	
1i9.	0001/0010/0100/l000	
22.0	0001/0011/0100/1000	BAND C
24.0	0001/0100/0100/1000	
27.0	0001/0101/0100/1000	
30.0	0001/0110/0100/1000	

*Each test equipment setup word consists of bits 0 through 15, numbered from left to right. This test route is the same as the olm&t test cable route.

Step 8. Change the differential simulator bit switch settings to those shown in table 5-13 for each of the remaining oscillators. Set the signal source assembly ATTENUATOR LEVEL SET control (see figure 3-3) for the oscillator in use to the amplitude shown in table 5-11 for V8 or table 5-12 for V7.

Step 9. Set the vvm (411A2) MODE switch to CHANNEL A and set the simulator bit switches as in step 5.

Step 10. Adjust the CHANNEL A ATTENUATOR control (on the front of the Signal Data Converter) to provide a reading of 65 millivolts on the vvm (41IA2).

Step 11. Set the vvm (411A2) phase VERNIER control to a phase reading of -2.8 degrees using the +6-degree phase scale on the vvm.

Step 12. Using the control words in table 5-13, verify the phase readings in table 5-11 (V8) or 5-12 (V7).

Step 13. Reconnect all cables to operating configuration. Reset the OLM&T FAULT control and BEAMFORM control on the somc control panel.

Step 14. Set the vvm controls as described in Step I of table 3-2.

5-14. Minimum Performance Standards.

Minimum performance standards for the olm&t group have been established in paragraph 5-8, Group Level Operational Tests. Performance is evaluated by making operational self-tests. Minimum performance required is successful execution of the four olm&t tests activated by the four controls on the somc control panel.

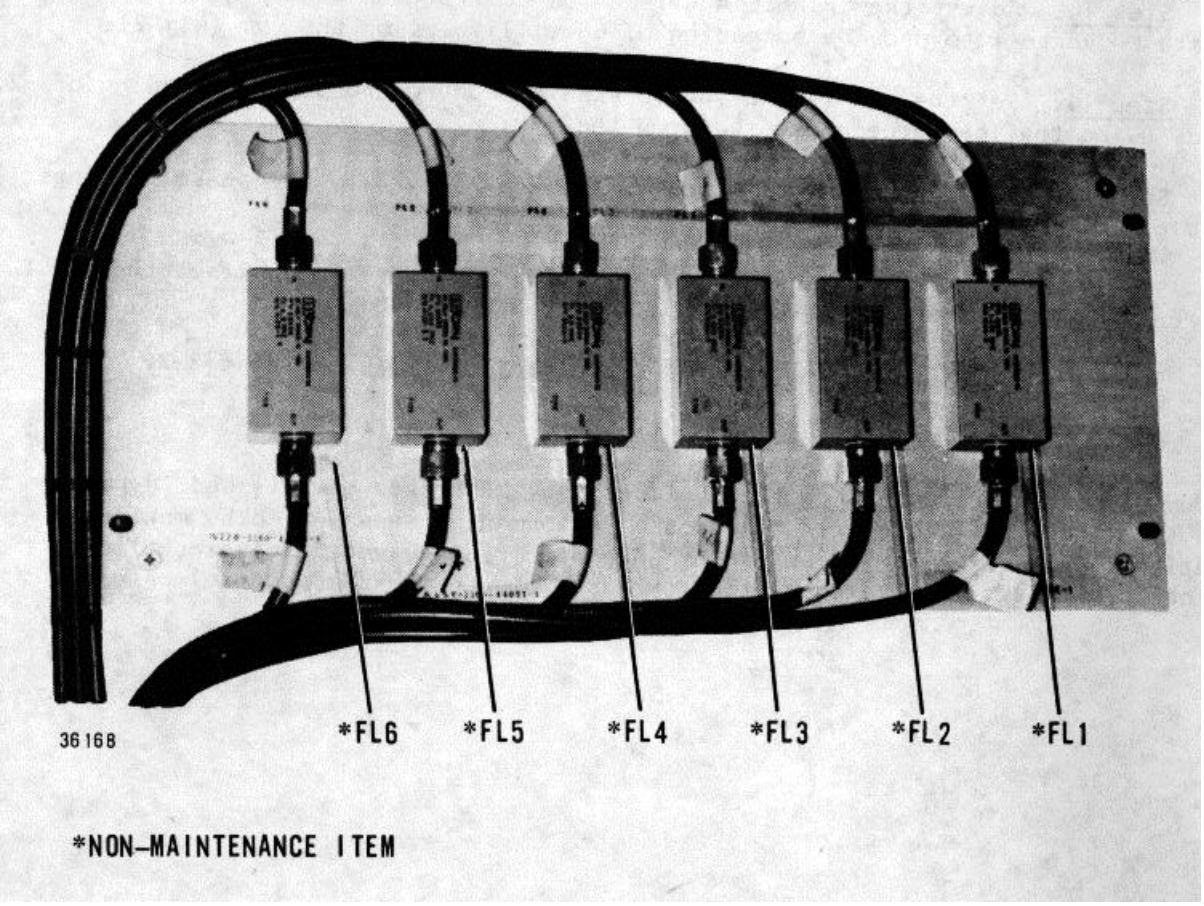
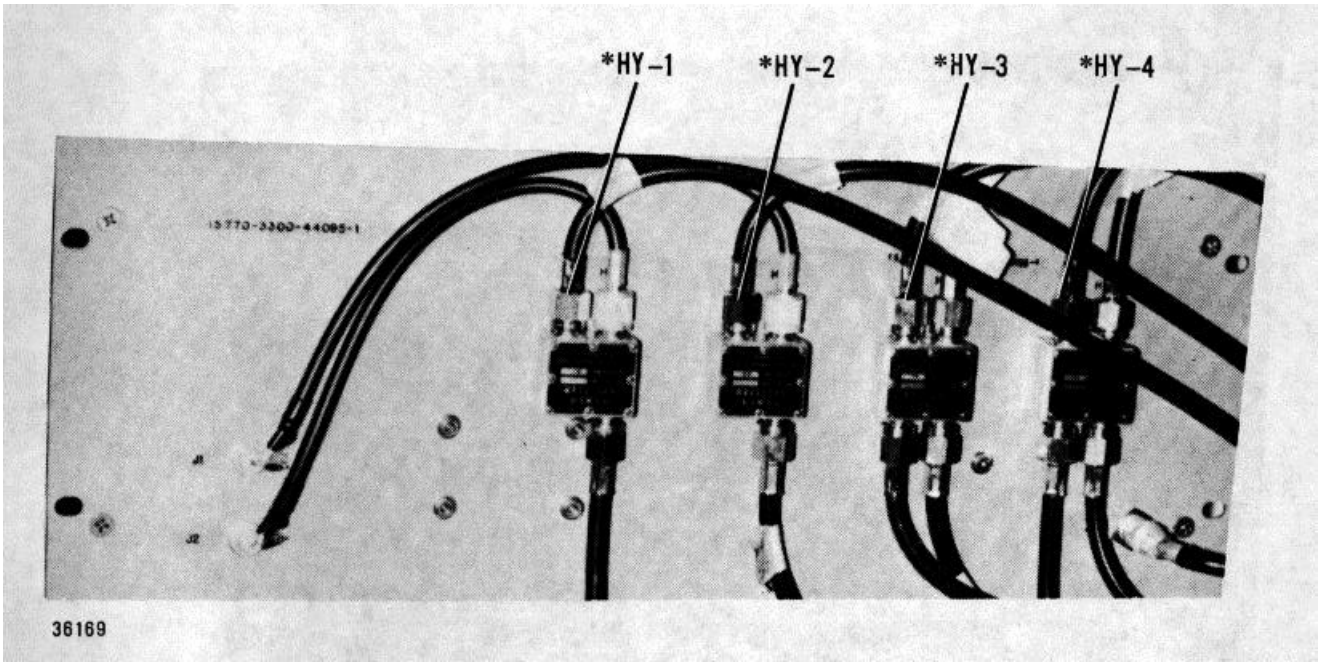
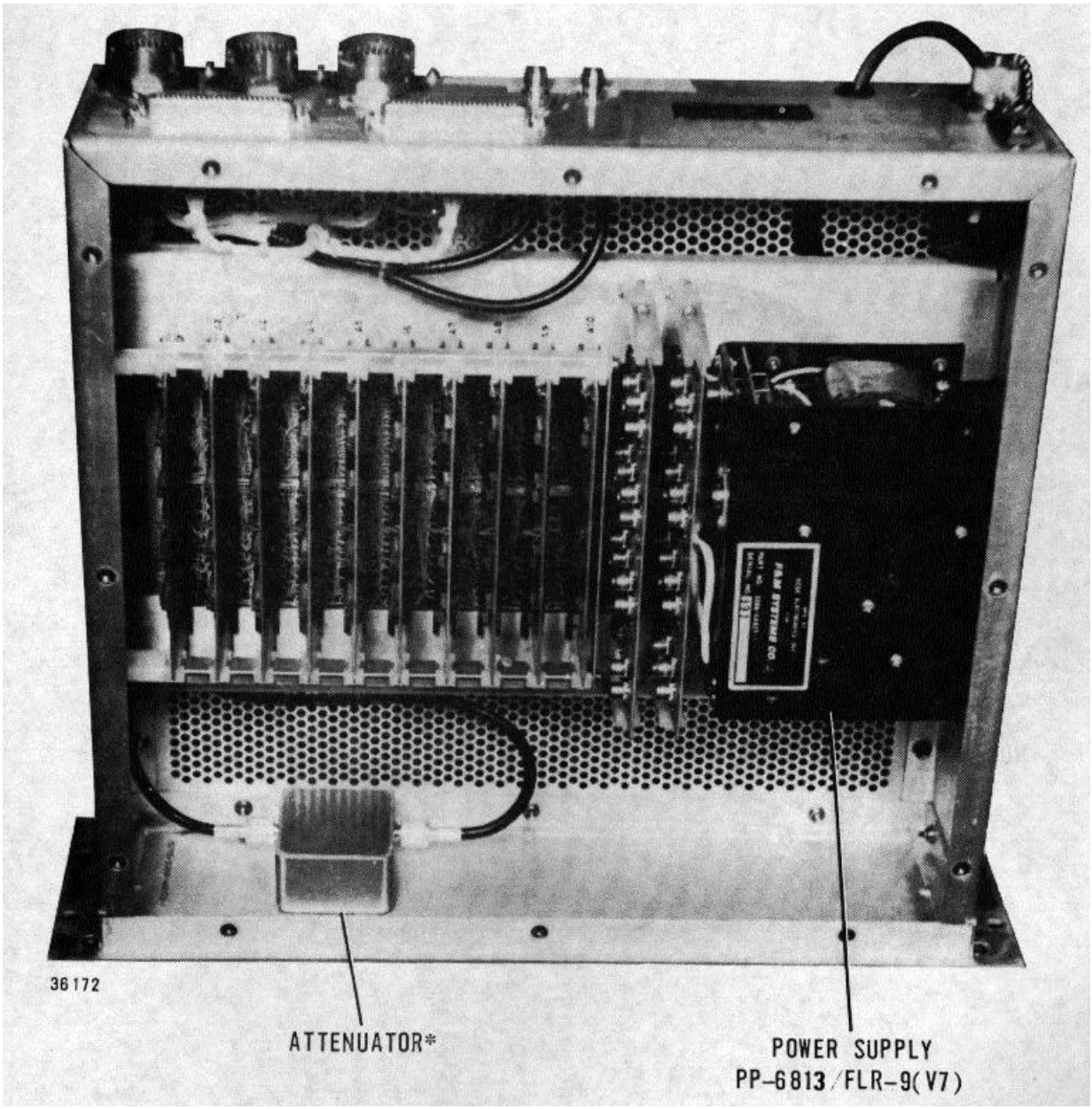


Figure 5-1. Filter Assembly Band Pass F-1337/FLR-9(V), F-1338/FLR-9(V), and F-1339/FLR-9(V). Typical 412A1, A2, and A3



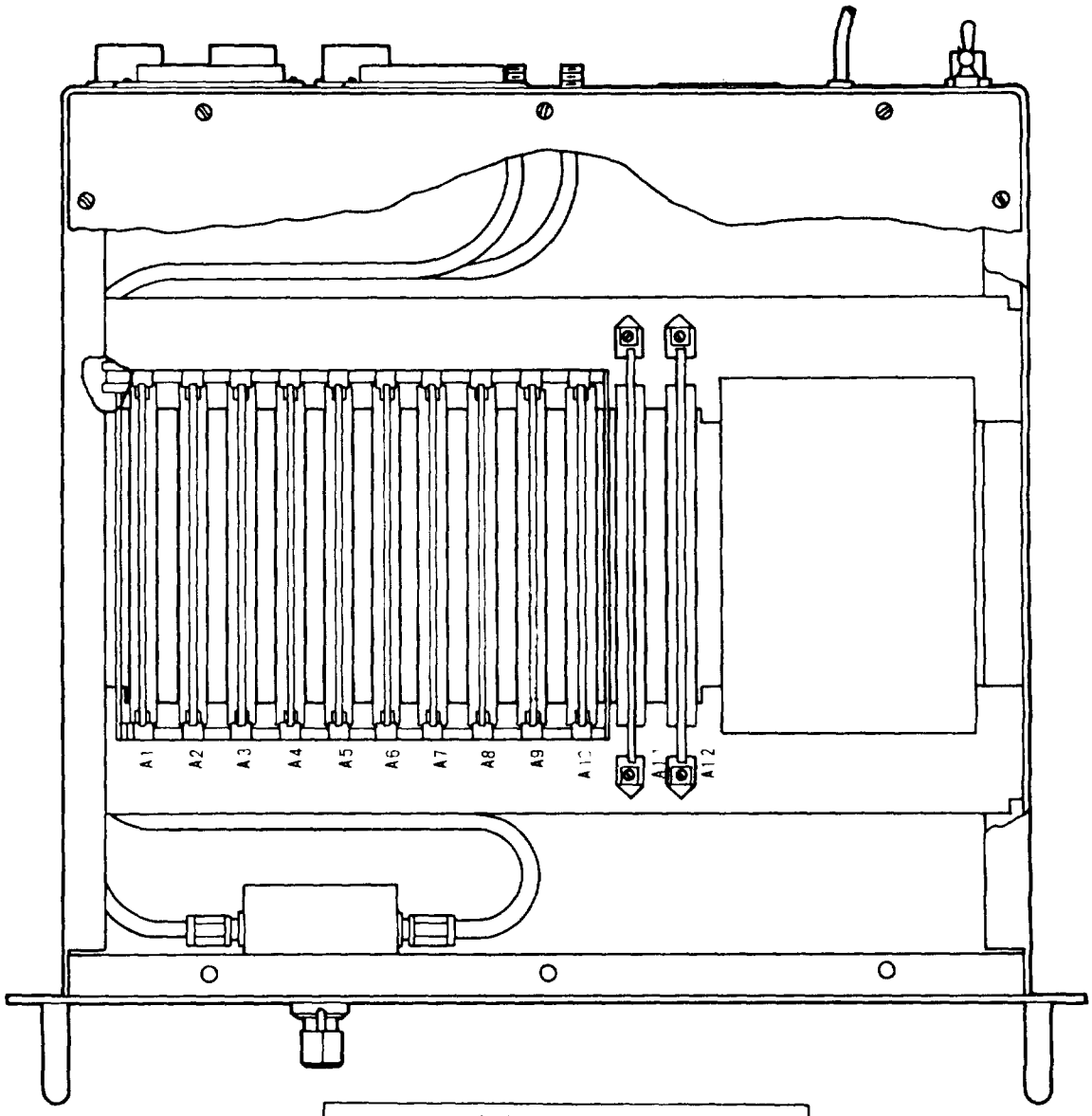
*NON-MAINTENANCE ITEMS

Figure 5-2. Divider Assembly, Power RF, CU2048/flr-9(V). 411A3



***NON-MAINTENANCE ITEM**

Figure 5-3. Top View, Signal Data Converter, CV-2977/FLR-9(V). 411A1



CROSS REFERENCE CHART	
CIRCUIT CARD LOCATION	CIRCUIT CARD PART NO.
A1	3300-46027-1
A2	3300-44044-1
A3, 4, 5, 6	3300-46028-1
A7	3300-44039-1
A8	3300-44040-1
A9	3300-44041-1
A10	3300-44042-1
A11	3300-44050-1
A12	3300-44049-1

39073

Figure 5-4. Component Board Location, Signal Data Converter

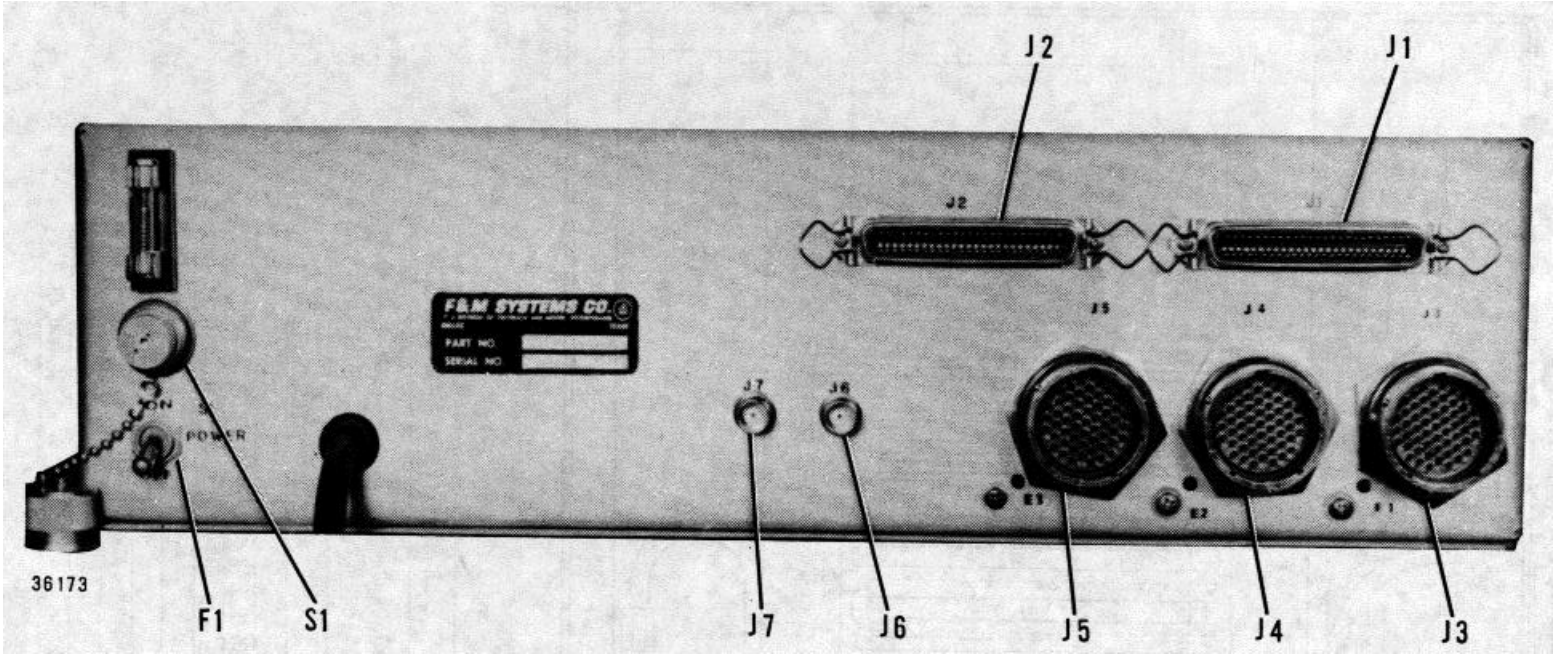


Figure 5-5. Rear View, Signal Data Converter, VC-2977/FLR-9(V). 411A1

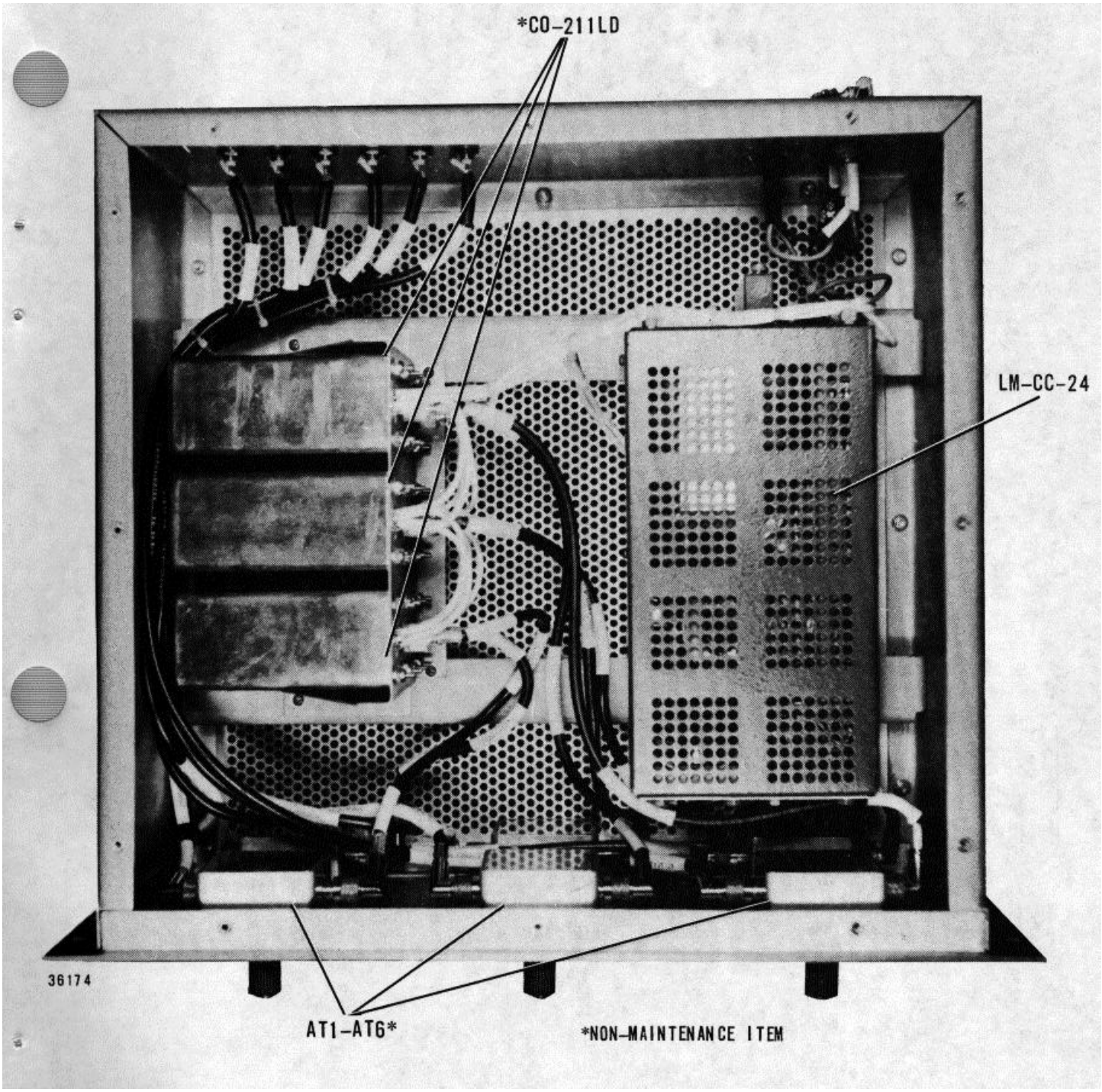


Figure 5-6. Top View, Test Oscillator Assembly, SG,-100/flr-9(V), SG-1002/FLR-9(V), AND SG-1003/FLR-9(V). Typical 413A1, A2, and A3

TERM	FUNCTION
1	DC INPUT (-)
2	DC INPUT (+) 24V
3	N C
4	N C
5	N C
6	N C
7	N C

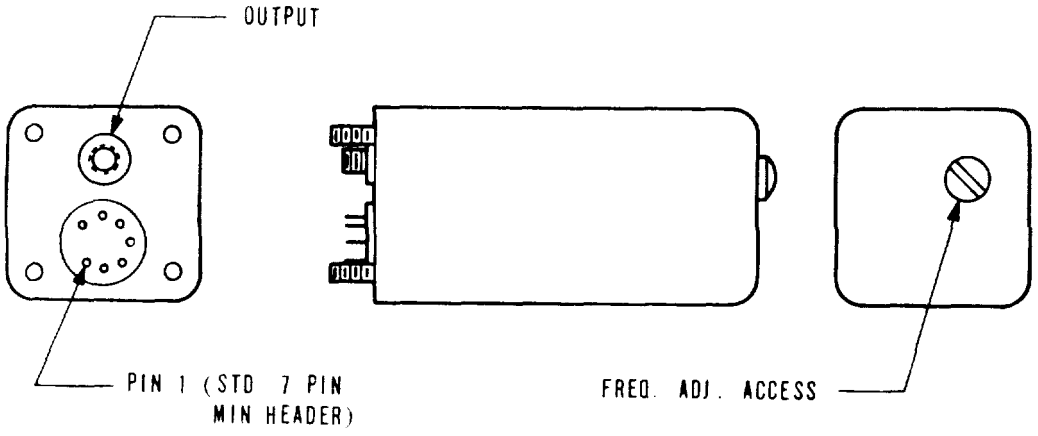


Figure 5-7. Assembly Drawing, Test Oscillator CO211LD

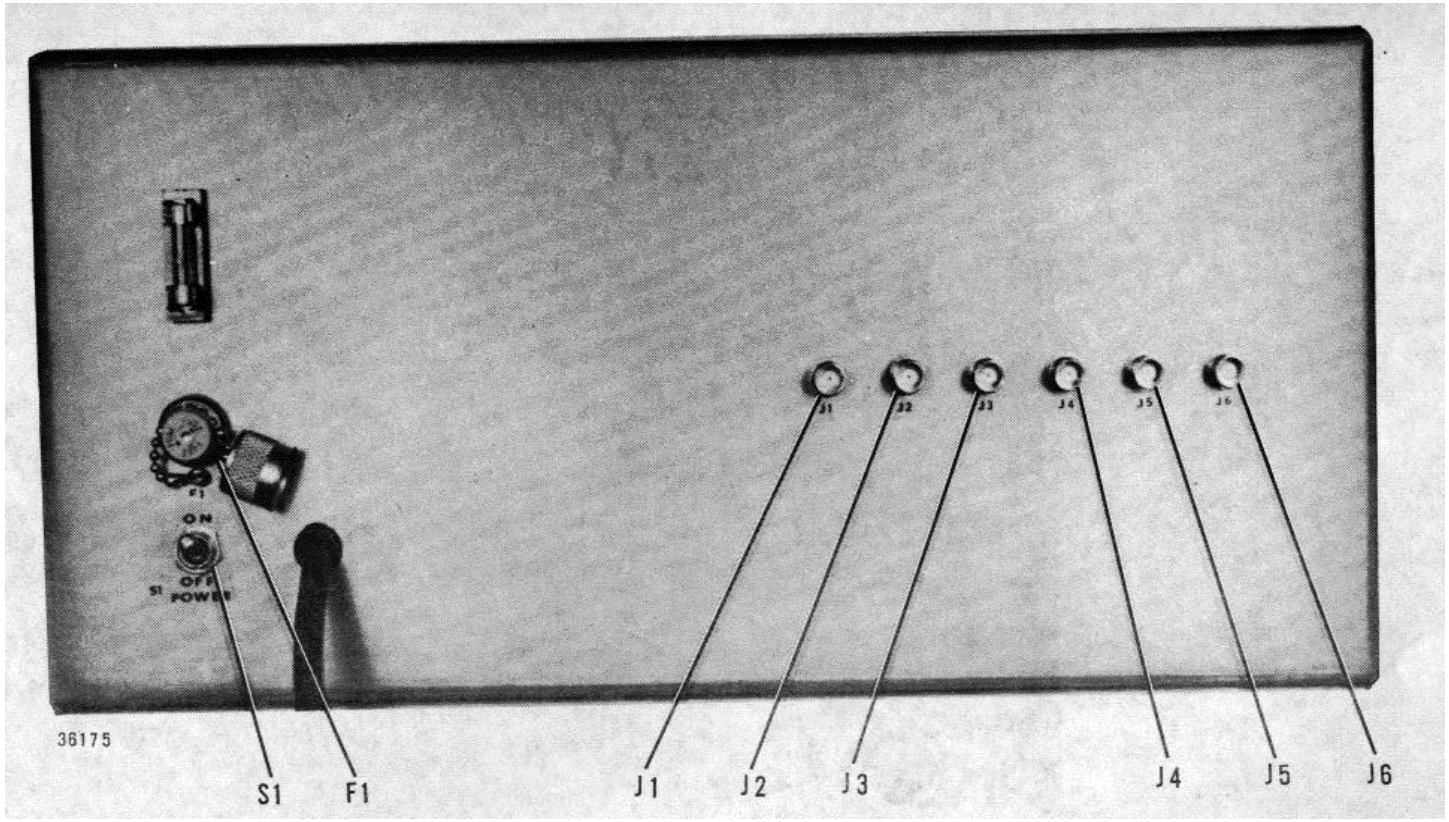


Figure 5-8. Rear View, Test Oscillator Assembly, SG-1001/FLR-9(V), SG1002/FLR-9(V), and SG-1003/FLR-9(V). Typical 413A1, A2, and A3.

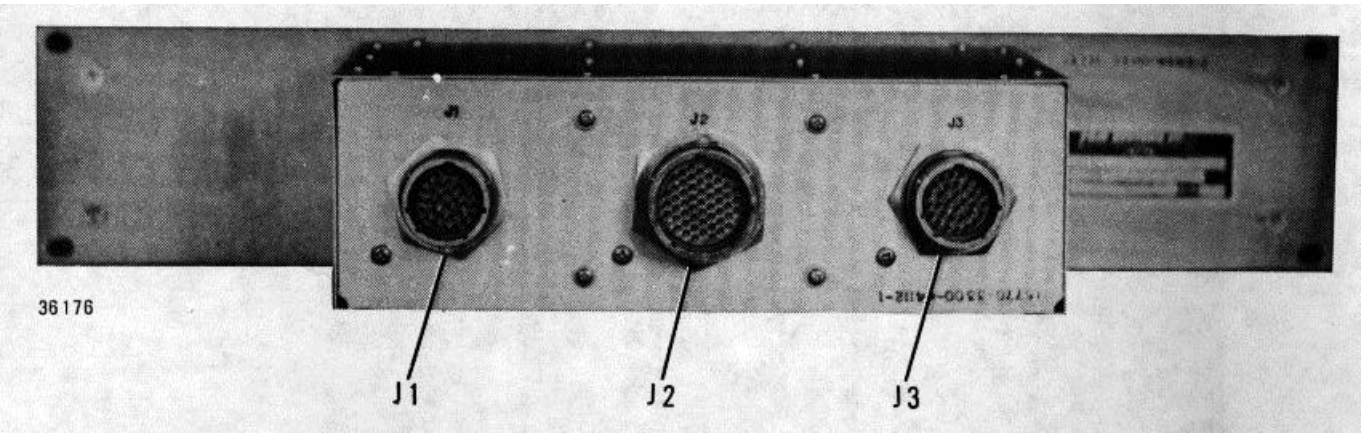


Figure 5-9. Rear View, Alarm Junction Box. 414A2

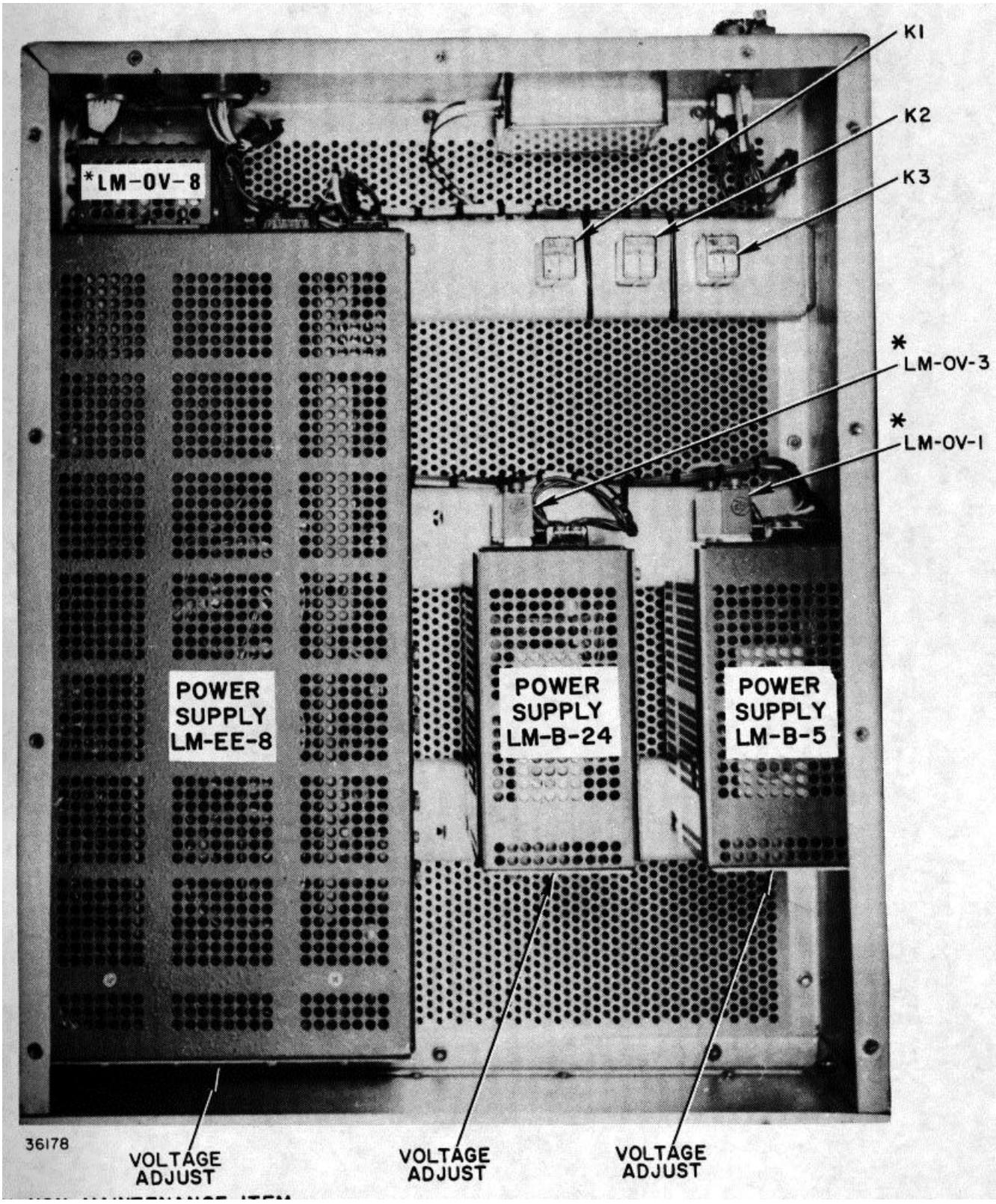


Figure 5-10. Top View, Power Supply PP-6814/FLR-9(v). 203A11(V8)

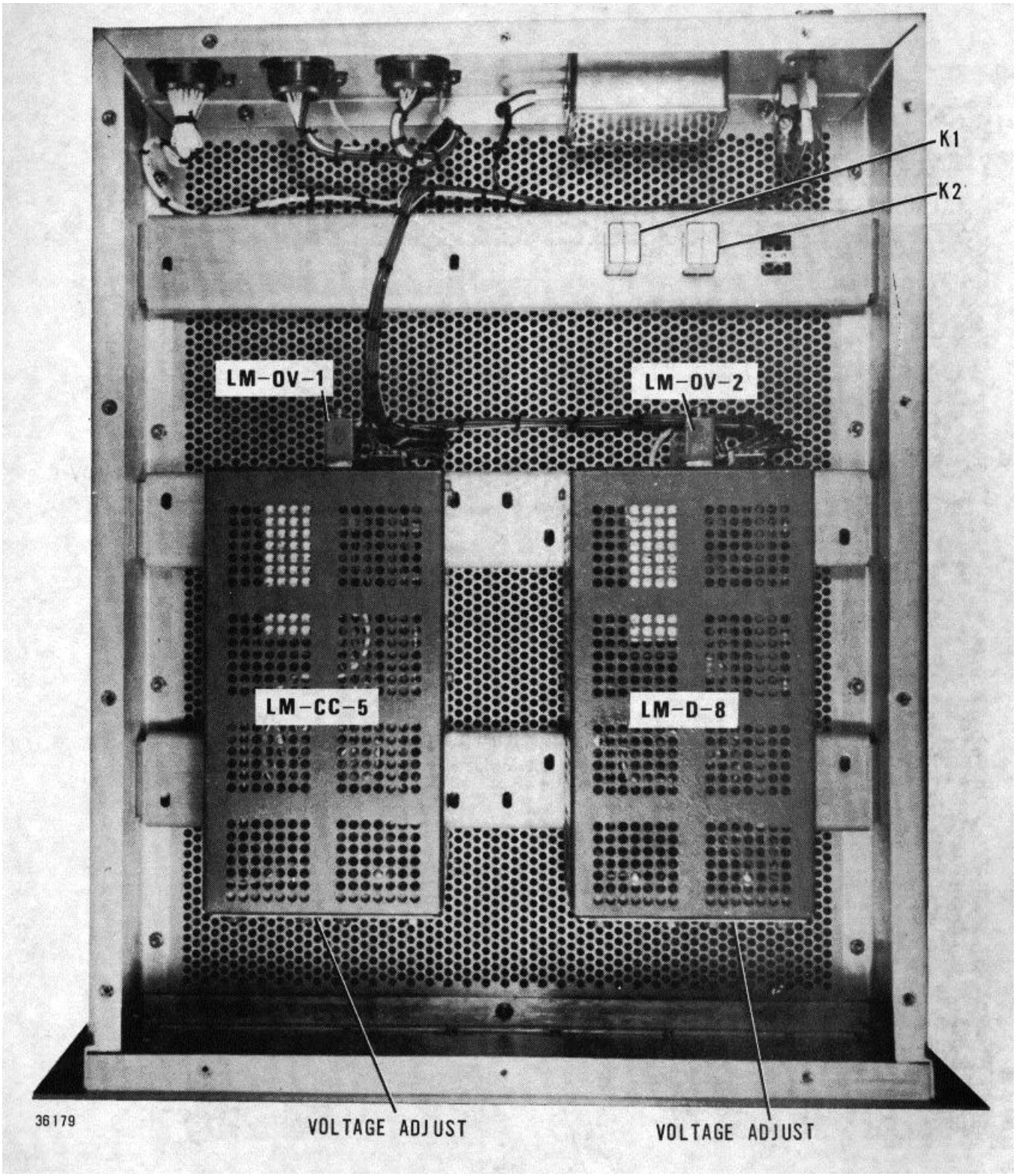


Figure 5-11. Top View, Power Supply, PP6811/FLR-9(v). 414A3

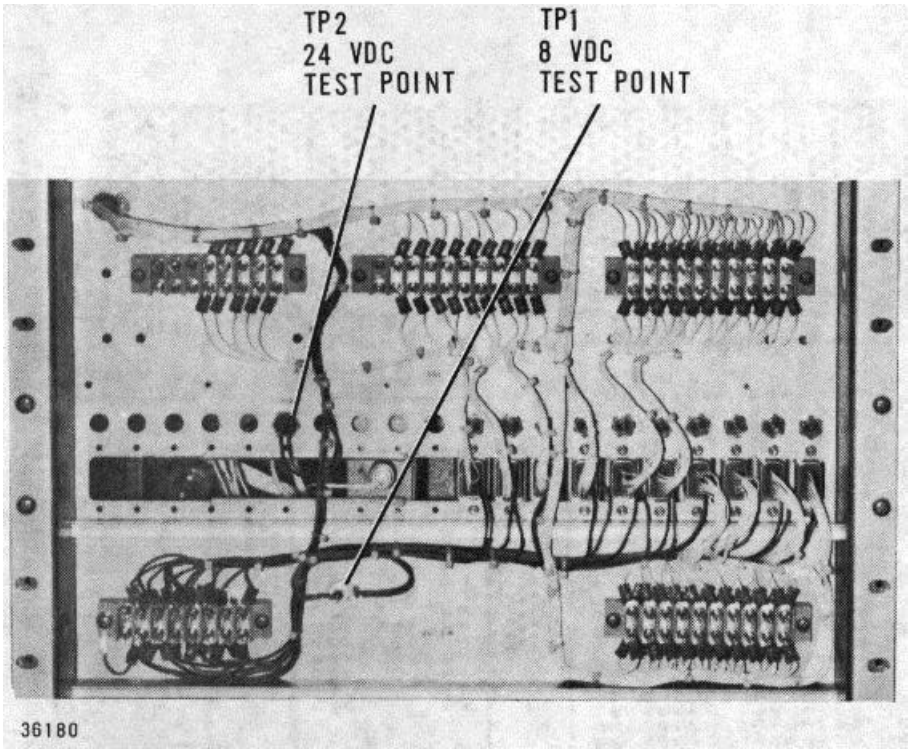


Figure 5-12. Group C Matrix, Power Supply Test Point Locations 414A13 (V8), 414A11(V7).

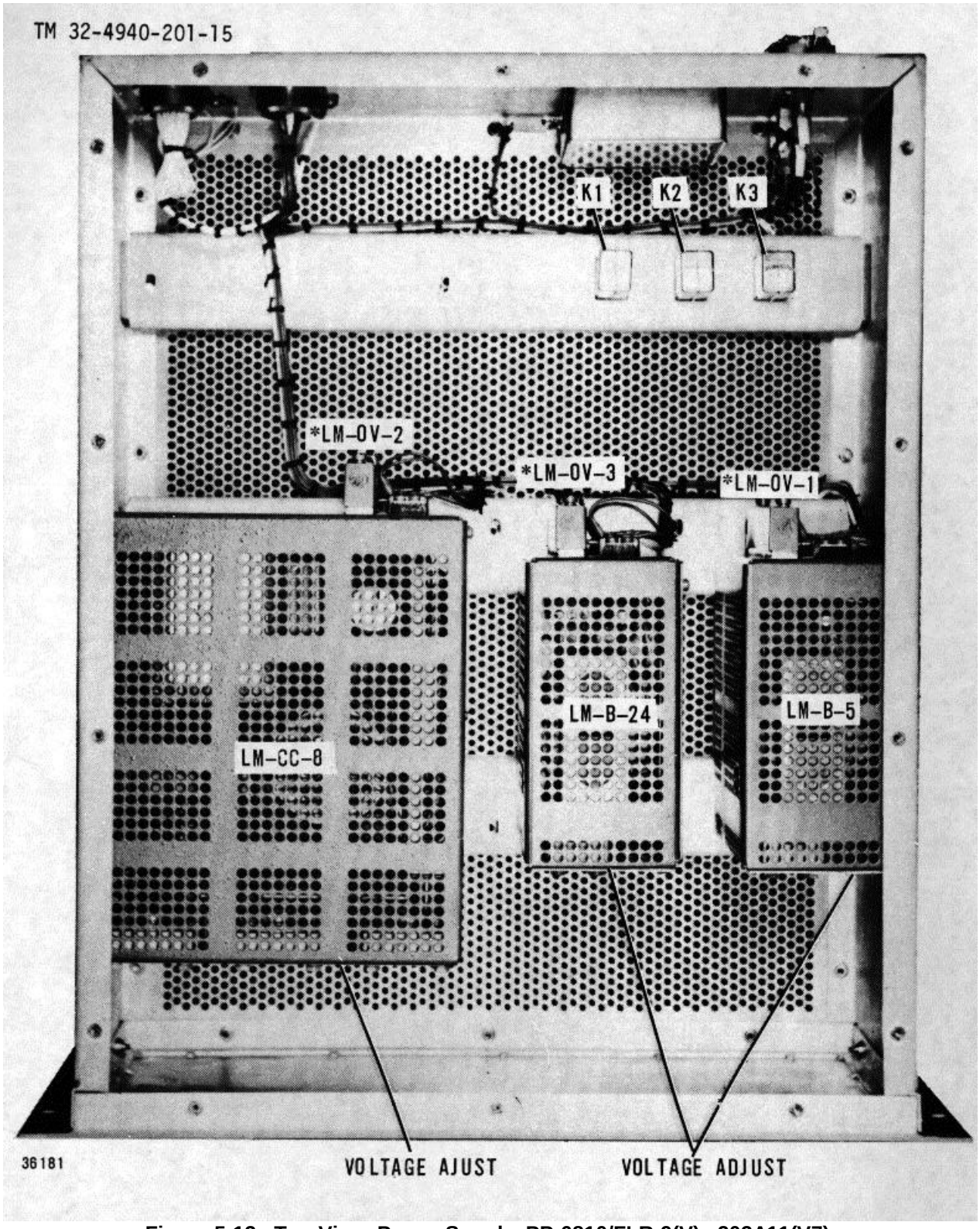


Figure 5-13. Top View, Power Supply, PP-6810/FLR-9(V). 203A11(V7).

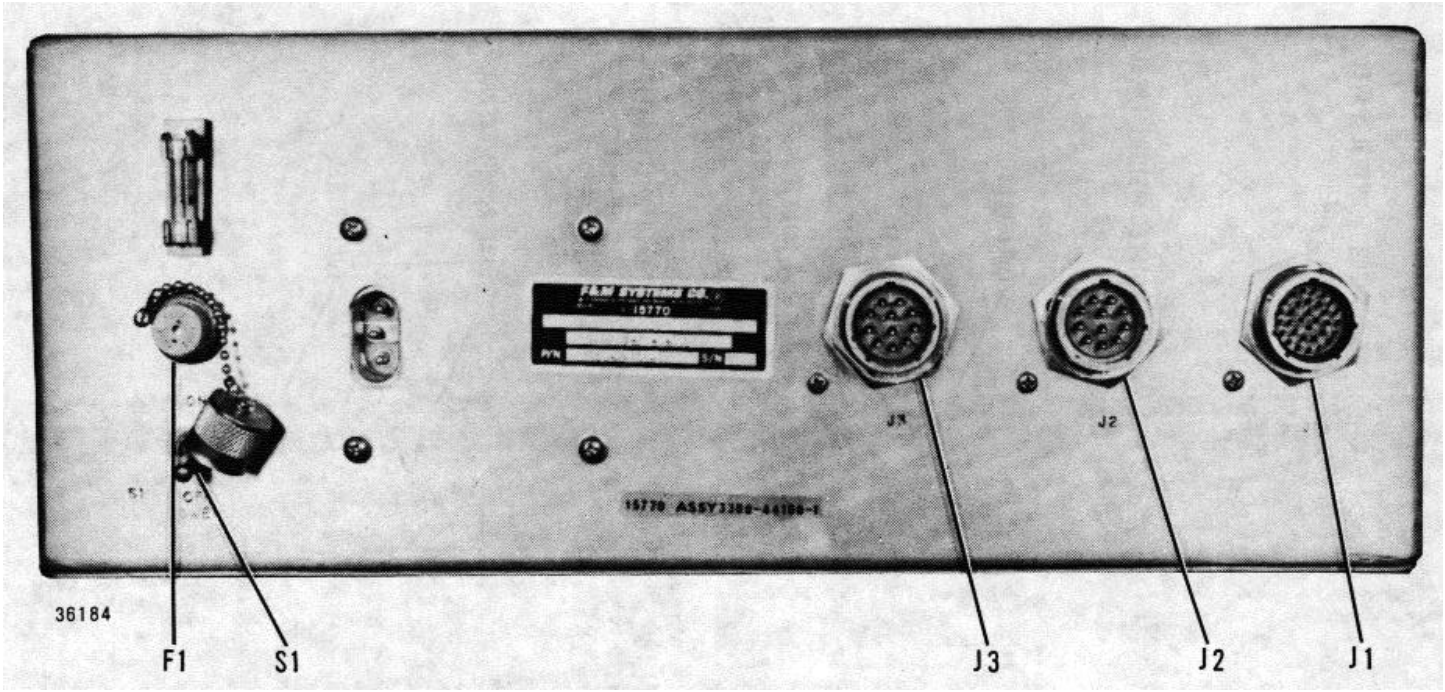


Figure 5-14. Rear View, Power Supply, PP-6811/FLR-9(v). 414A3

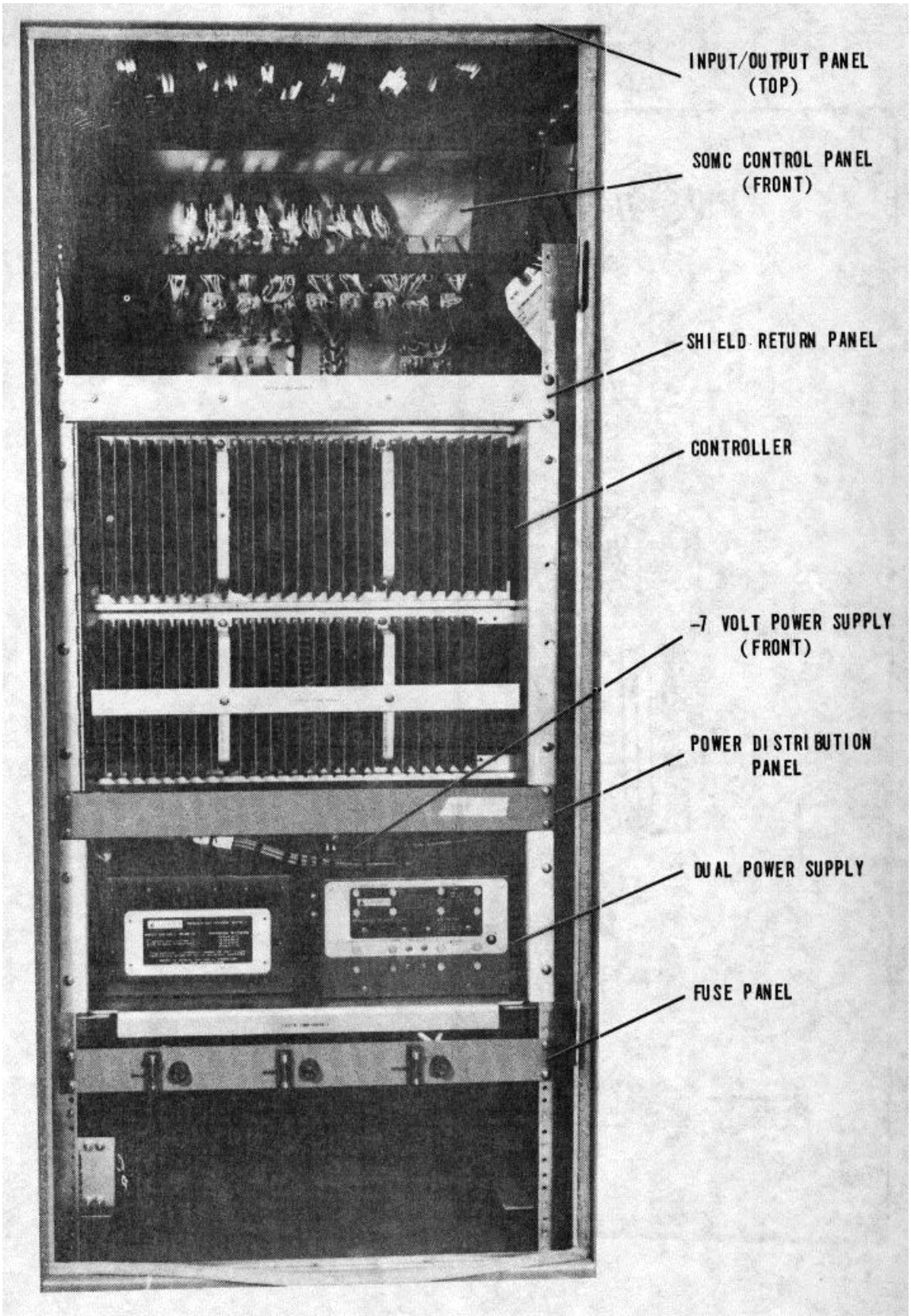
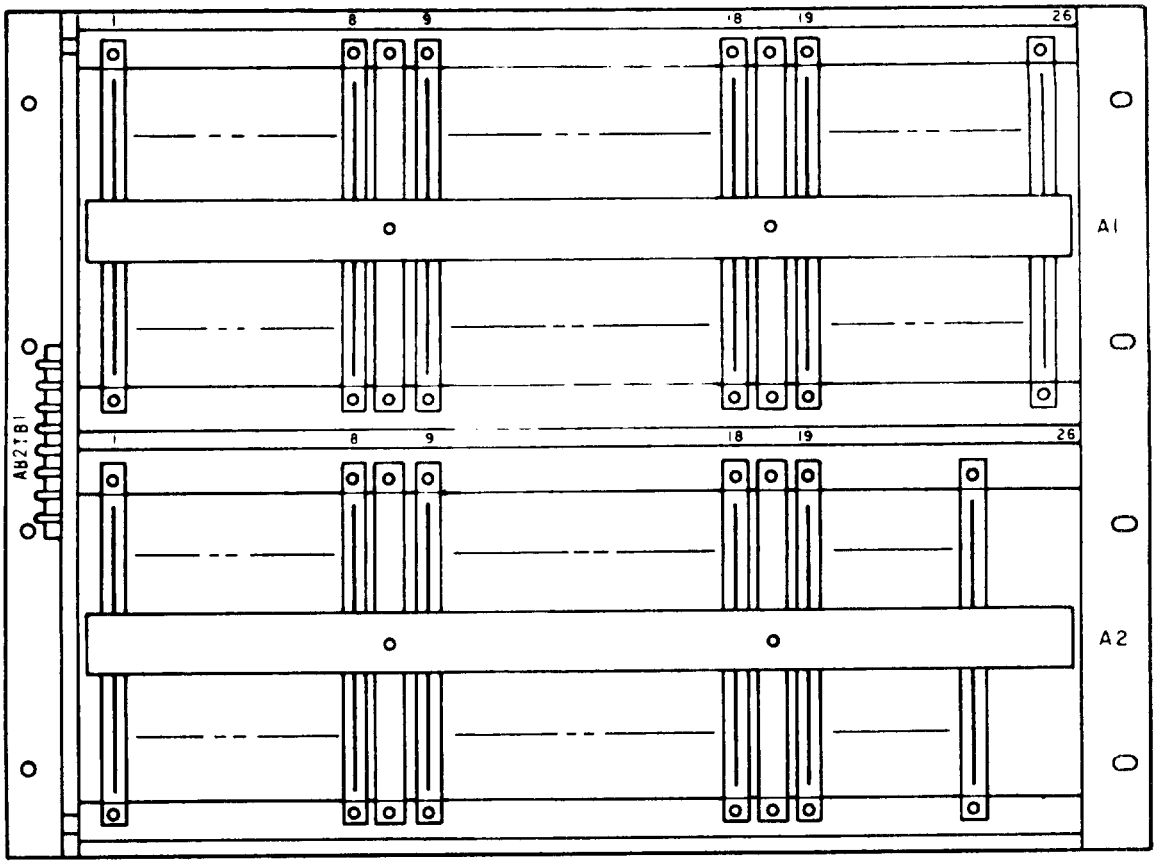


Figure 5-15. Somc, Rear View



CROSS REFERENCE LISTING	
CIRCUIT CARD PART NO.	CIRCUIT CARD REF DES
3300-46027-1	A216, 217, 220, 221
3300-46075-1	A101
3300-46008-1	A102
3300-46013-1	A104, 106
3300-46012-1	A103, 105, 115, 116
3300-46083-1	**
3300-46028-1	A214, 219
3300-46017-1	A112, 113, 114, 123
3300-46093-1	A222, 223, 224
3300-46077-1	A108, 110, 212, 124
3300-46078-1	A109, 111, 213, 125
3300-46079-1	A107, 126
3300-46080-1	A204, 208, 211
3300-46081-1	A117
3300-46082-1	A118 THRU A122

** REF DES ARE A201, 202, 203, 205, 206, 207, 209, 210, 215, &218.

39072

Figure 5-16. Assembly Drawing, component Location, Somc Controller

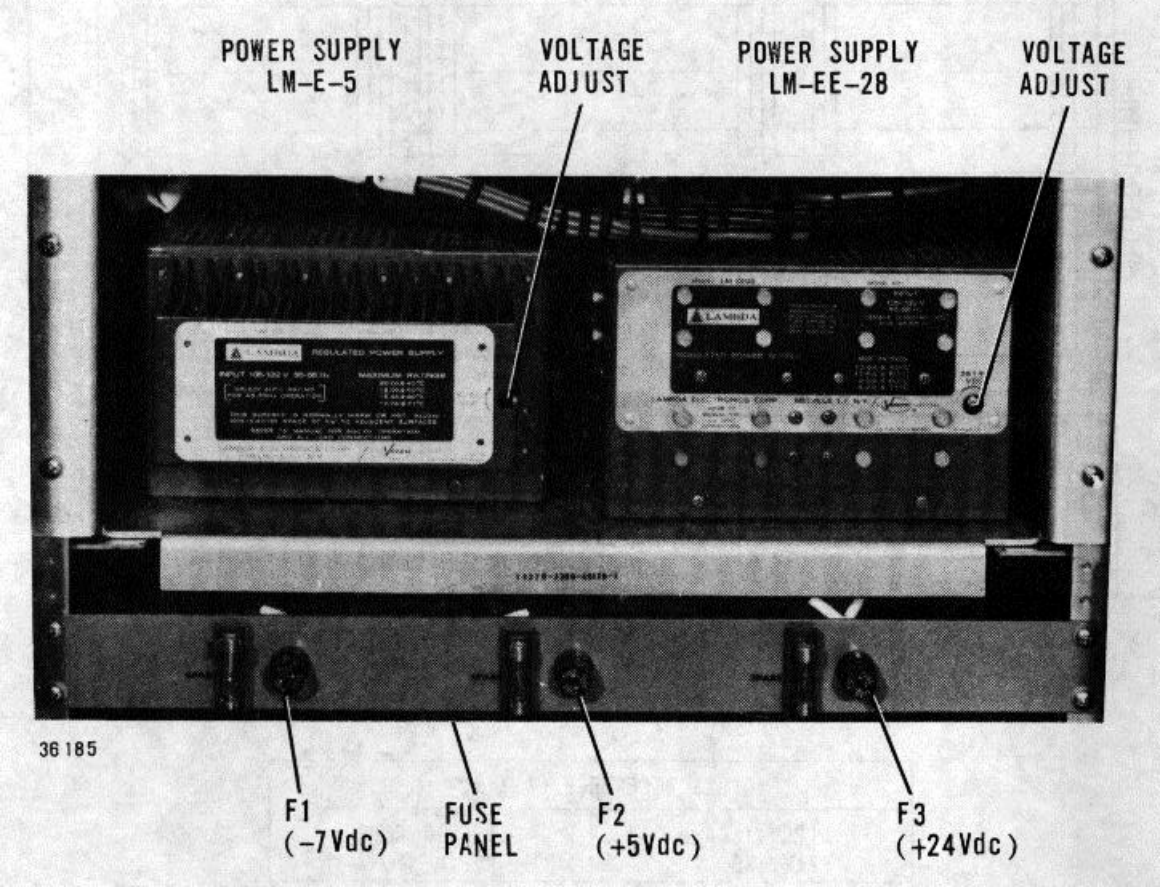
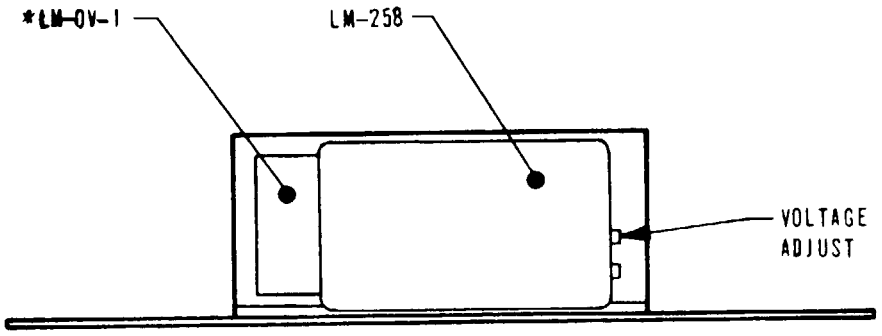


Figure 5-17. Somc Dual Power Supply and Fuse Panel Assemblies, 217AB4 and AB5.



* NON-MAINTENANCE ITEM

Figure 5-18. Power Supply assembly PP6890/FLR-9(V), Location 217A3, Top View

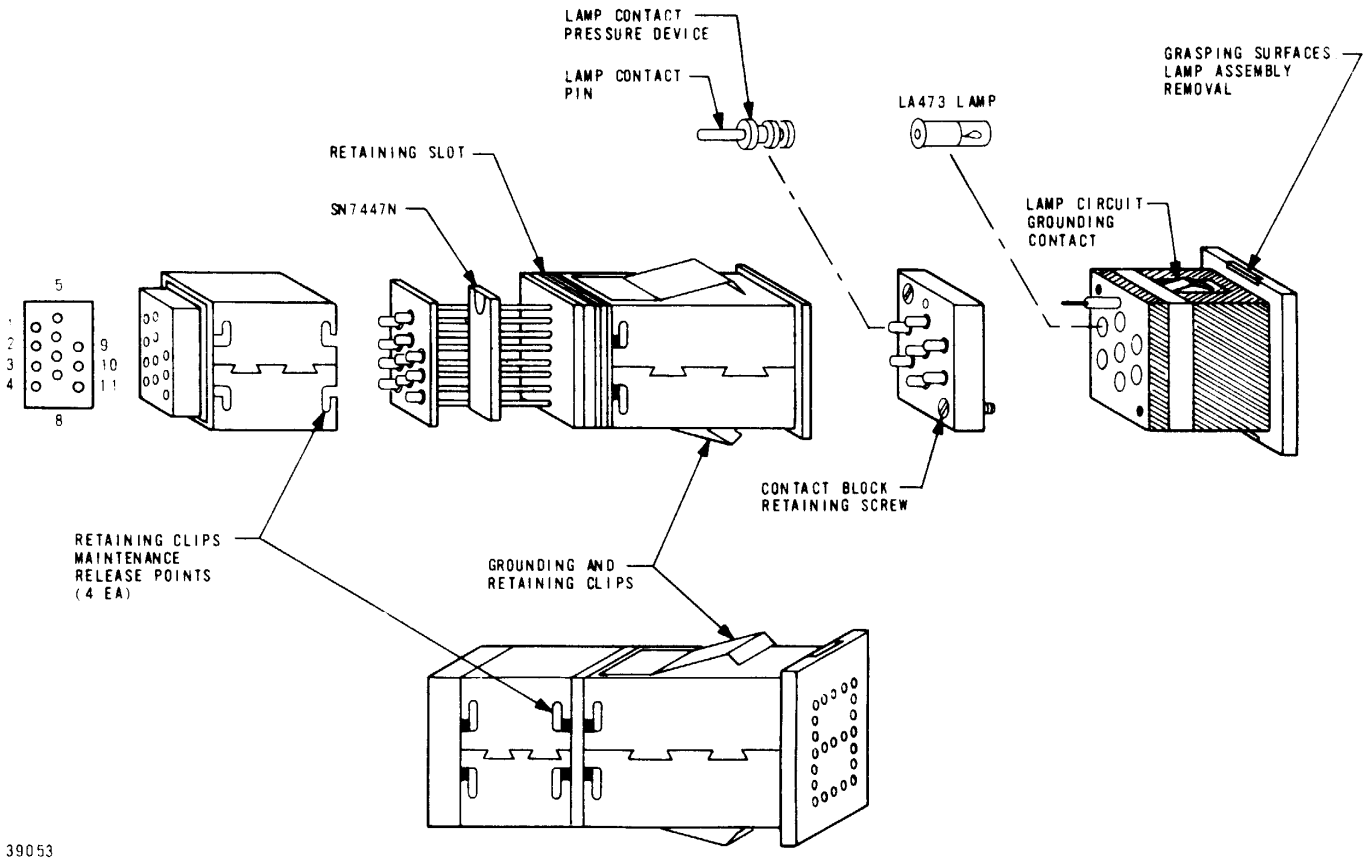


Figure 5-19. Indicator, Somc DSI-DS9, Assembly Drawing

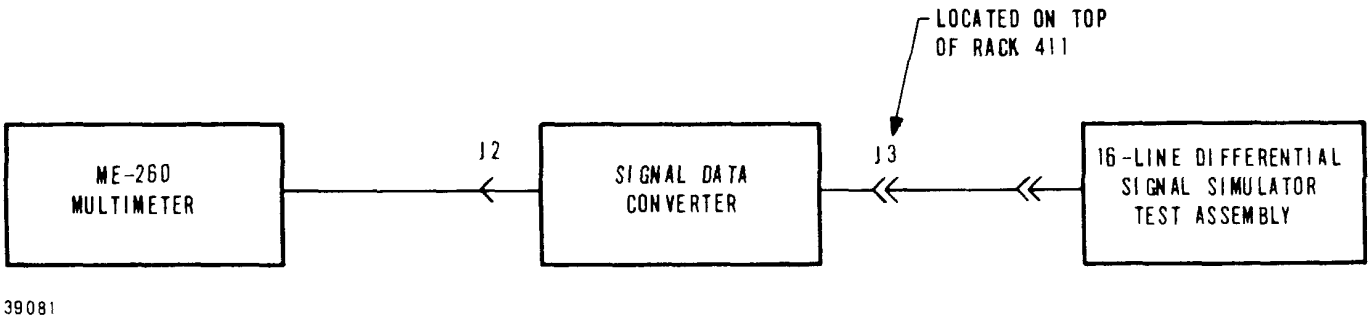


Figure 5-20. Test Setup, Frequency Range and Apc Unlock Circuits, Signal Data Converter

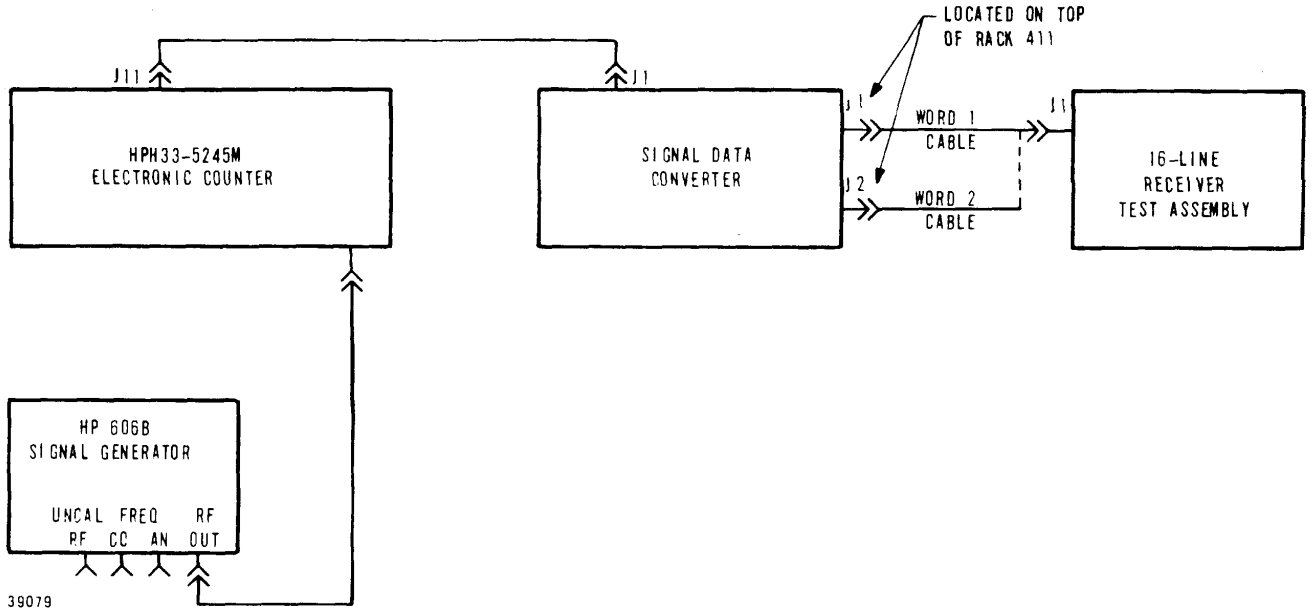


Figure 5-21. Test setup, Electronic Counter circuits, Signal Data Converter

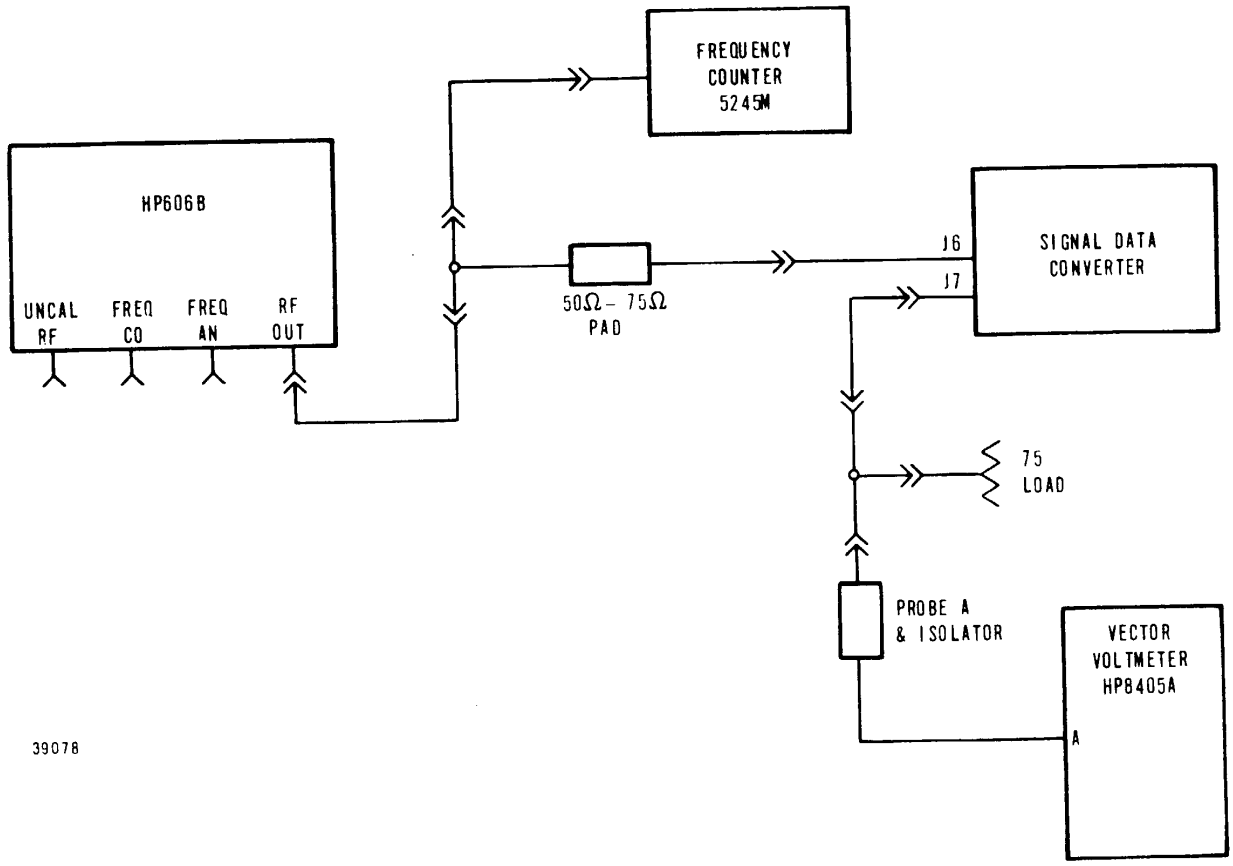


Figure 5-22. Test Setup, Attenuator Test, signal Data Converter

SECTION VI

DEPOT INSPECTION STANDARDS

6-1. Scope.

The material in this section is to provide test instructions for evaluating equipment that has been repaired to insure that performance meets the original specifications.

6-2. Tests.

A list of the tests performed and test equipment required is given in table 6-1 for each equipment for planning purposes.

6-3. Test Procedures. (See table 6-1 and figures 6-1 and 6-2.)

a. Inspection of Generator, Signal SG-1OO1/FLR-9(V), SG-1002/FLR-9(V), and SG-1003/FLR-9(V). This assembly is the olm&t signal source for bands A, B, and C test signals.

1. Preliminary Requirements.

(a) Primary Power. Primary power is 120 volts ac +10O percent, single-phase, 47 to 63 Hz at 2.0-ampere minimum capacity.

(b) Warm-up. The unit is to be allowed a 24-hour warm-up period before beginning tests.

(c) Test Equipment. Table 6-1 lists test equipment required for each sequential step. Figures 6-1 and 6-2 show test equipment connections.

(d) Initial Adjustment. After the warm-up period and before testing is begun, check the output of the power supply contained in the signal generator assembly. If necessary, adjust to 24 volts dc *0.5 volts.

Table 6-1. Test Equipment Required

Sequence	Test	Test Equipment
(a) Steps 1 through 4	Oscillator frequency check	Frequency Counter HP5245A
(b) Steps 5 through 8	Output level check	Attenuator HP355C Vector Voltmeter HP8405A
(c) Steps 9 through 11	Attenuator calibration check	Attenuator HP355C Vector Voltmeter HP8405A
(d) Steps 12 through 15	Harmonic and spurious signal performance check	Spectrum Analyzer HP8553B

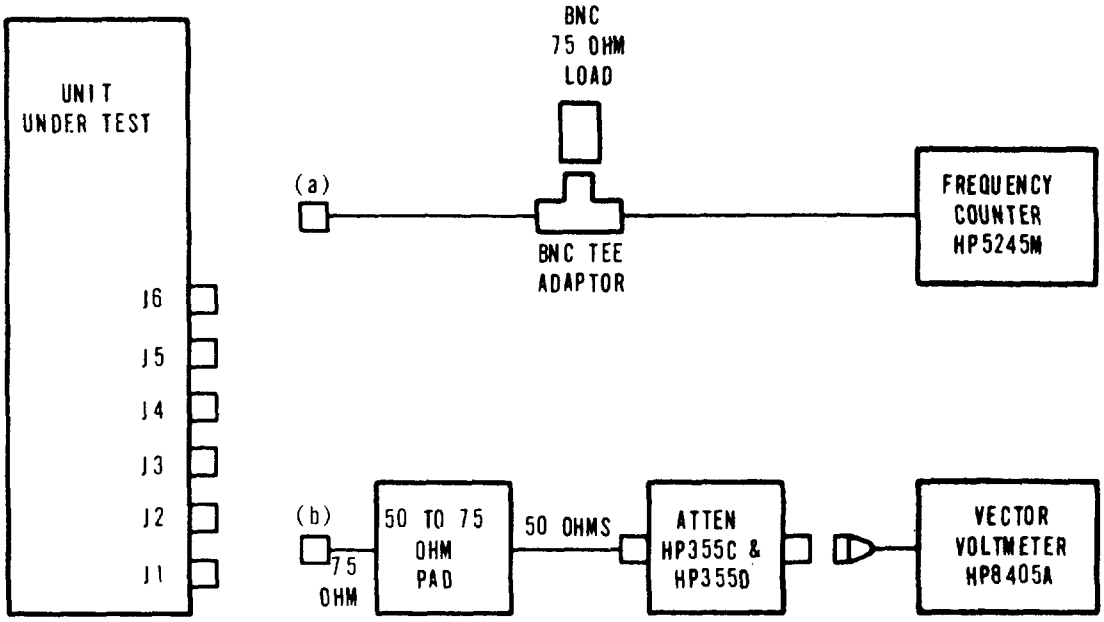


Figure 6-1. Test Connections, Frequency and level Checks

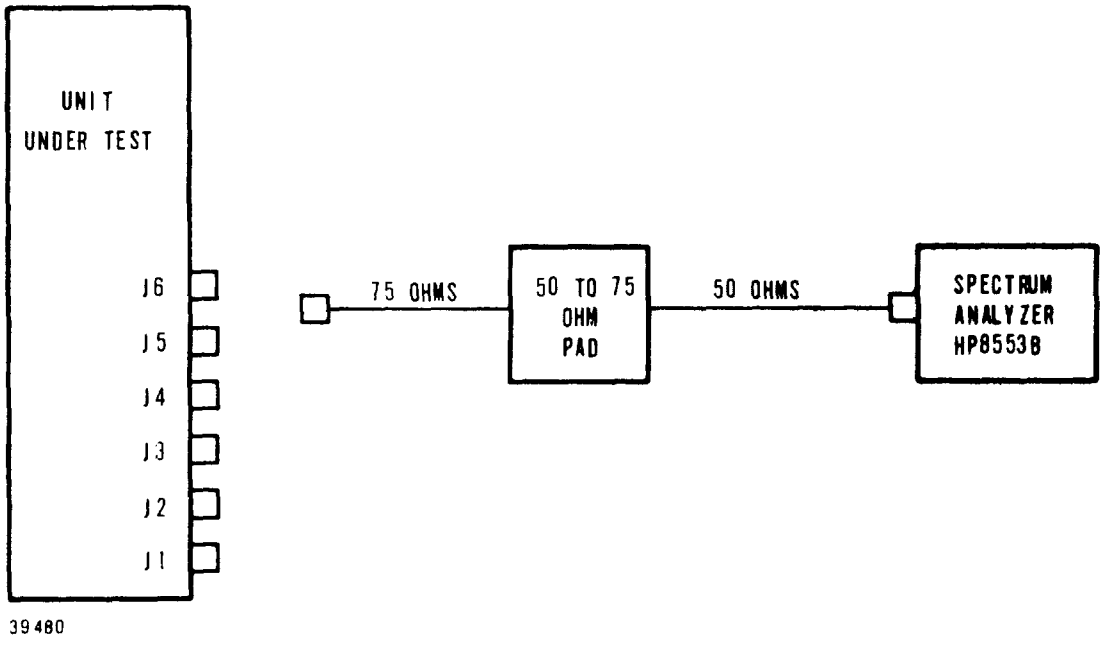


Figure 6-2. Harmonic and Spurious Signal Check Test Connections

2. Unit Test.

(a) Oscillator Frequency Check.

Step 1. Connect the test equipment as shown in figure 6-1(a), using the frequency counter. Allow a 20-minute frequency stabilization period after each oscillator is connected to a load.

Step 2. Connect each oscillator output to the frequency meter and allow it to stabilize.

Step 3. Read the output frequency. Each output frequency is to be within one part per million of the specified output.

Step 4. If the frequency is out of specification limit, adjust the oscillator frequency change control (see figure 5-7).

(b) Output Level Check.

Step 5. Connect the test equipment as shown in figure 6-1(b), using the vvm.

Step 6. Set the HP355C Attenuator as needed to obtain an on-scale reading.

Step 7. With each oscillator front panel attenuator set to 10 dB, connect the HP355C input to each of the output connectors Jl through J6. The output of each connector is to be less than +12 dBm.

Step 8. With each attenuator set at minimum, the output power is to be not less than +18 dBm Check each output by connecting the input of the HP355C to Jl through J6.

(c) Attenuator Calibration Check.

Step 9. Connect the test equipment as shown in figure 6-1 using the vvm.

Step 10. Set the front panel attenuator for each oscillator under test to its minimum position and adjust the HP355C Attenuator to provide a convenient zero on the vvm.

Step 11. Move each oscillator attenuator through its range. Note correlation between attenuator dial setting and vvm reading. Indicated level should correspond with measured level within ±i dB.

(d) Harmonic and Spurious Signal Performance Check.

Step 12. Connect the test equipment as in figure 6-2.

Step 13. At each output, set the oscillator attenuator to mid-scale and tune the spectrum analyzer to the oscillator output frequency.

Step 14. Adjust the analyzer controls until the displayed signal appears to just touch the top horizontal graticule of the analyzer display. (More amplitude than this causes the analyzer to produce intermodulation products greater than -70 dB down.)

Step 15. Tune through the frequency range of 1.5 to 30 MHz and measure all harmonics and spurious signals present. If any signals are present, they are to be at least -65 dB below the fundamental signal.

b. Inspection of Power Supply Assemblies PP-6811/FLR-9(V), PP-6810/FLR-9(V), and PP-6814/FLR-9(V). These assemblies are power sources for the olm&t switch matrices A, B, and C.

1. Preliminary Requirements. (See tables 6-2 and 6-3, and figures 6-3 and 6-4.)

(a) Primary Power. Primary power is 120 volts ac t10 percent, single-phase, 47 to 63 Hz, and 4.0-ampere capacity.

(b) Warm-up. The assembly under test is to be energized for 15 minutes preceding tests.

(c) Test Equipment. Table 6-2 lists test equipment required for each sequential step. Figures 6-3 and 6-4 show test equipment connections.

(d) Initial Adjustments. After warm-up, measure the output of each supply in the assembly. If necessary, adjust to within +0.25 volts of the rated output voltages (see table 6-3). At this time, the overvoltage protectors may be checked by turning the output voltage of the power supply up until the voltage is limited by the protector. This voltage limit is to be +1.0 volts above the rated voltage. If not, adjust the overvoltage level control on that circuit assembly.

Table 6-2. Test Equipment Required

Sequence	Test	Test Equipment
Initial adjustments, Step 2.	Output voltage check	Differential Voltmeter, Fluke 853A.
Initial adjustments, Step 5.	Line regulation	Variable ac power source 108-120-volt ac at 4 amperes capacity with monitor voltmeter.
Steps 6, 7, and 8.	Voltage ripple	Oscilloscope HP140A
Steps 2 and 4	Output load regulation	Resistive loads (see table 6-4).
Steps 10 and 11	Relay operation	Multimeter, Simpson 260-S

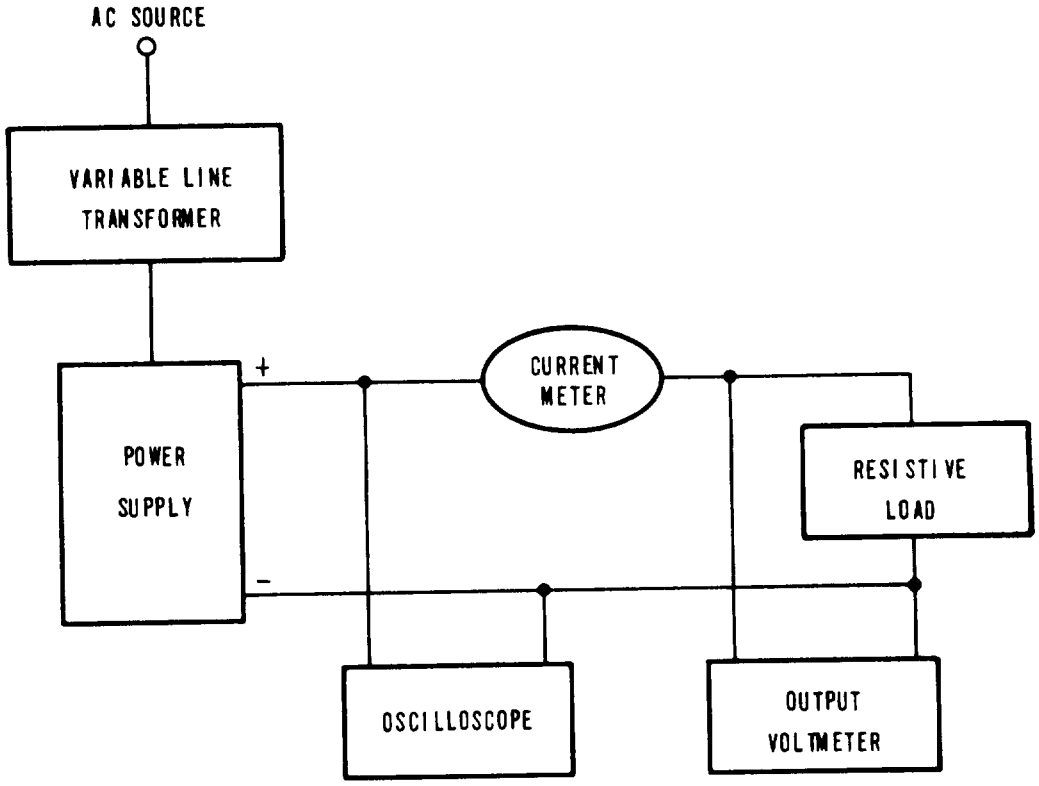


Figure 6-3. Test Equipment setup

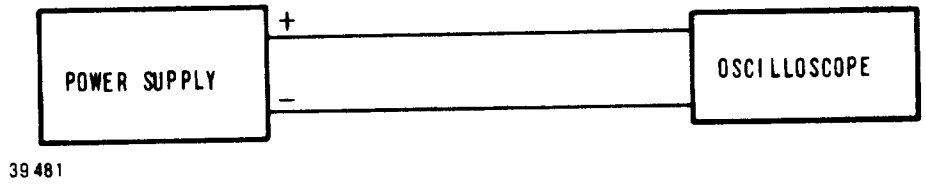


Figure 6-4. Test Equipment Setup, Ripple Test

Table 6-3. Output Voltage Ratings

Assembly	PSI Rated Output Voltage	PSI Output Pins	PS2 Rated Output Voltage	PS2 Output Pins	PS3 Rated Output Voltage	PS3 Output Pins
PP-6811/ FLR-9(V) (Power Supply Assembly Number I	(LM-CC-8) 8 volts dc	J2-D(+), J2-E J3-D(+),J3-E	(LM CC-5) 5 volts dc	J2-G(+), J2-H J3-G(+),J3-H	NONE	NONE
PP-6810/ FLR-9(V) (Power Supply Assembly Number 2	(LM-D-8) 8 volts dc	J2-D(+),J2-E	(LM-B-24) 24 volts dc	J2-A(+) ,J2-B	(LM-B-5) 5 volts dc	J2-G(+),J2-H
PP-6814/ FLR-9(V) (Power Supply Assembly Number 3	(LM-EE-8) 8 volts dc	J2-D(+),J2-E	(LM-EE-24) 24 volts dc	J2-A(+) ,J2-B	(LM-EE-5) 5 volts dc	J2-G(+) ,J2-H

2. Unit Test. (See tables 6-4 and 6-5.)

(a) Current Output Test.

Step 1. Connect the test equipment as shown in figure 6-3 (see table 6-2).

Step 2. While monitoring the output voltage and current, increase the output loading until the output voltage and current begin to drop back, indicating that the maximum regulation limit has been reached. Compare the output current obtained within the acceptable values in table 6-4.

Step 3. Connect the equipment as shown in figure 6-3, using the variable line transformer and oscilloscope.

Step 4. Adjust the unit under test to the rated current given in table 6-4.

Step 5. Vary the input power to +10 percent (108 to 132 volts ac). Output voltage change must not exceed +0.5 volt dc.

Step 6. Check ripple and noise components on the oscilloscope. Ripple and noise may not exceed 5 millivolts peak-to-peak about the rated voltage.

(b) Ripple and Noise Test, No Load.

Step 7. Connect the equipment as in figure 6-4, using the oscilloscope.

Table 6-4. Acceptable Current Outputs

NOTE
Unless otherwise specified, use resistive load rated 400 watts.

Assembly	PSI		PS2		PS3	
	Current Minimum	Voltage Minimum	Current Minimum	Voltage Minimum	Current Minimum	Voltage Minimum
PP-6811/FLR-9(V) (Power Supply Assembly Number 1)	10 Amps	7.7 Volts	8 Amps	4.8 Volts	NONE	NONE
PP-6810/FLR-9(V) (Power Supply Assembly Number 2)	6 Amps	7.7 Volts	*1 Amps	23.76 Volts	3 Amps	3 Amps
PP-6814/FLR-9(V) (Power Supply Assembly Number 3)	25 Amps	7.7 Volts	*1 Amp	23.76 Amps	3 Amps	4.8 Volts

*Use 50-watt resistive load for this measurement.

Table 6-5. Power Supply Alarm Relay Output Pins

Assembly	PS1		PS2		PS3	
	Relay	Output Pins	Relay	Output Pins	Relay	Output Pins
PP-6811/FLR-9(V) (Power Supply Assembly Number 1)	K1	J1-e&f	K2	J1-b&c	NONE	NONE
PP-6810/FLR-9(V) (Power Supply Assembly Number 2)	K2	J1-D&E	K1	J1-G&H	K3	J1-A&B
PP-6814/FLR-9(V) (Power Supply Assembly Number 3)	K2	JI-D&E	K1	J1-G&H	K3	J1-A&B

Step 8. Measure the peak-to-peak value of ripple and noise for each unloaded output. Ripple and noise must not exceed 5 millivolts peak-to-peak.

(c) Relay Operation. (See table 6-5.)

Step 9. Connect the equipment as shown in figure 6-4, using the ohmmeter.

Step 10. With the ohmmeter connected across the output contacts of connector Jl and the power supply energized, note that the contacts are opened. (See table 6-5.)

Step 11. Deenergize the power supply. Note that the contacts are closed in the alarm condition.

c. Inspection of Converter Signal Data CV-2977/FLR-9(V). Depot inspection of the signal data converter is the same procedure as paragraph 5-ll.a (Signal Data Converter Troubleshooting). Acceptable performance is the proper result of each action performed.

GLOSSARY

A

A/D Analog-to-digital.

ANTENNA ARRAY Circular disposed antenna elements tuned to a particular band of frequencies.

ANTENNA ELEMENT A single element used in an antenna array.

ASCII American Standard code for information interchange (See LEC Leap Assembler Manual).

ASR Automatic send/receive.

AZIMUTH Angular direction clockwise from true north.

B

BCD Binary coded decimal in which lines are weighted 8, 4, 2, and 1.

BEAM ASSIGNMENT TABLE A table contained in the computer program which defines rf beams available to a radio receiver as selected by a bsu/biu.

BEAMFORMER A device which forms a directional broadband rf signal.

BLOCKING Inhibiting use of paths between Al and A2 or A2 and A3 switch matrix submatrices.

BOOTSTRAP Simple initial computer routine which enables the computer to initiate loading of larger program from an external device.

BORESIGHT ELEMENT Antenna element to the right of (even elements) or on (odd elements) the received radio beam center line.

BSU/BIU Beam select unit/Beam Identification unit.

BUFFER Circuit which stores data or provides load isolation for signal lines.

C

CABLE SCANNER Multiplexer which routes input signals to the computer.

CARD FILE Assembly containing circuit cards, card jacks and interconnecting wiring.

CCD Cyclic coded decimal in which the bits change In segments of one each per word.

CENTRAL BUILDING Building located in center of antenna array.

CPU Central processing unit; the computer minus input/output accessories.

COUPLING Connection of the same rf input beam to two or more receivers that are connected to the output ports in a common A3 submatrix.

D

DECOUPLING Use of STAGE REMOVED command to clear switch map table of paths of receivers who are coupled to the same faulty rf beam In the A3 submatrix to allow the operator to obtain an alternate path to the receiver.

DECODER Circuit for conversion between numerical systems (such as bcd to decimal).

DFG Direction finding group DIAGNOSTIC ROUTINE Special computer program which senses and defines faults.

DIRECTIONAL COUPLER Passive device which provides low impedance in the desired direction and high Impedance in all other directions to rf signal inputs.

DIU Digital interface unit.

DOT-OR Logical OR function not present in any one circuit; occurs because of the nature of connected outputs from other circuits.

DAUGHTER BOARD Pcb which mounts on a motherboard.

DUMP Output computer memory contents to some output device such as a tty.

E

EAI External address in; computer output signal which enables transfer of address between two computers.

ECI External command input; computer output signal which enables routing of a command to the computer.

ECO External command output computer output signal which defines the nature of i/o bus signal.

EDI External data input; computer output signal which enables routing of data to the computer.

EDO External data output; computer output signal which defines the nature of i/o bus signal.

EMI Electromagnetic interference.

ESI External status input; computer output signal which enables routing of status signal to the computer.

EXCLUSIVE-OR Logic circuit which produces a high output when one (not more than one) input is high.

G

Goniometer Rotating device which forms a directional rf beam from received signals.

H

HANDOVER Occurs when the primary computer relinquishes control of the system to the on-line standby computer.

HEXADECIMAL The numbering system in the computer program which uses 16 as a radix. The 16 combination of bits in a 4-bit group provides decimal digits of O through 9 and A through F.

I

INTERFACE Circuits between the computer and other equipment necessary for routing, storage, format/level conversion, or special processing.

INTERRUPT Causes computer to stop doing a relatively unimportant routine and perform one of higher priority; after interrupt, computer returns to previous task.

I/O Input and output.

I/O BUS Computer's connection to external equipment.

I/O BUS SWITCH Routes signals from/to active computer to/from external devices.

I/O DRIVER RECEIVER Line driver and signal converter.

IPDC Internal programmed data channel.

J-K FLIP-FLOP Flip-flop which can be operated asynchronously, like an R-S flipflop, and/or synchronously with a clock, J, and K inputs. The J and K inputs are sometimes provided with AND gates.

L

LATCH Storage register.

LEC Lockheed Electronics Company LINE DRIVER Circuit which produces balanced signals in response to single-ended logic signal.

LINE RECEIVER Circuit which produces a single-ended logic signal in response to a balanced input signal.

LOAD To enter the program into the computer.

LOGIC Electronic circuits or groups of circuits designed to make a discrete response to a particular combination of input signal levels.

LOGIC ERROR Program detects that set is executing at an illegal location or detects that a cpu controlled parameter is out of limits.

M

MAGNETIC TAPE CONTROLLER Electrical interface between computer and tape unit; it provides buffering, motion control, and error control.

MATRIX An array of crosspoints in which any point may be addressed by a system of coordinates.

MATRIX MULTIPLEXER Multiplexer which routes computer outputs to external equipment.

MCC Memory control chassis associated with MAC 16 computer.

MDC Multiplex data channel; a high-speed portion of the computer pdc i/o structure.

MEMORY EXPANSION CHASSIS Holds all computer memory in excess of 8192 words, and also interface logic circuits.

MONITOR BEAM A directional beam, selected with automatic selected directivity.

MOTHERBOARD A circuit card where other circuit cards are physically mounted.

MULTIPLEXER Signal selector or router which acts as a multiple,-pole rotary switch, under external (computer) control.

MUX Multiplexer.

N

NAND Circuit which produces a low output only when all inputs are high.

NOR Circuit which produces a low output when any (one or more) inputs (including all inputs) are high.

O

OLM&T On-line monitor and test function of the monitor and test group.

OMNIBEAM A non-directional beam.

OPTICAL ENCODER Produces a ccd output to define the direction of the goniometer beam.

P

PDC Programmed data channel; part of computer i/o structure.

PERIPHERAL EQUIPMENT Equipments interfacing with a single unit of equipment for control or signal application purposes.

PROGRAM Set of instructions, constraints, and information stored in computer memory which enables a computer to perform a particular task (or series of tasks).

PROGRAM AZIMUTH SHEET List of beams assigned to a given bsu/biu.

R

REDUNDANT (MUX, CPU, etc) Energized standby equipment identical to that equipment presently in control.

REED SWITCH MATRIX Any of three test matrices in the monitor and test group designated matrix A, matrix B, and matrix C and the special project switch matrix.

RFI Radio frequency interference.

RFSM Radio frequency switch matrix; a part of the rf matrix group.

ROUTINE A particular part of an overall program which performs a certain function within the program.

S

SAMPLING MATRIX, OLM&T A reed switch mounting assembly contained as a part of, or all of, an olm&t test matrix designated matrix A, matrix B, or matrix C.

SECTOR BEAM A directional beam with manually selected directivity.

SINGLE-SHOT Circuit which produces a single fixed duration pulse in response to an input signal.

SOMC Supervisory operation maintenance console.

SPECIAL PROJECT BSU/BIU A beam select unit which selects any bands and beams without requiring a beam assignment table.

STANDBY The non-controlling computer of the two provided. When on-line, it is continuously accepting data from the primary computer; can assume control immediately upon request.

SUBMATRIX Consists of a number of circuit cards, each with multiple inputs and a single output, arranged in such a manner as to provide a two-dimensional (X, Y) array of switchable rf crosspoints.

T

TABLE An array of data, constraints, or references in the computer program.

TELETYPE CONTROLLER LEC provided circuit card which provides signal buffering for a teletype under computer control.

TRANSMISSION LINE TUNERS Coaxial line stretcher.

TSA Computer program instruction.

TTY Teletypewriter.

TUNNEL Underground access between operating building and central building housing connecting cables.

V

VVM - Vector voltmeter.

W

WATCHDOG TIMER - A periodically reset counter which provides an interrupt to the opposite computer if not reset within 150 milliseconds.

X

X-PT - A crosspoint in the switch matrix.

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INDEX (Continued)

INDEX (Continued)

INDEX (Continued)

SECTION VII

MAINTENANCE ILLUSTRATIONS

7-1. Scope.

This section consists of illustrations referenced in sections IV, V, and VI. As a minimum, the following illustrations are contained within this section.

a. Overall schematic or logic diagram
b. Primary power distribution
c. Dc power distribution

7-2. Logic Circuit Diagram Labeling. (See figure 7-1.)

Labeling used on the Countermeasures Receiving Set AN/FLR-9(V7)/(V8) logic diagrams is shown in figure 7-1. The labeling identifies the signal origin and destination by use of the diagram sheet number and applicable drawing coordinates. Signal levels (high or low) are identified by use of a P or N following the signal name signifying a high or low level signal, respectively. Within each logic symbol, tagging lines are used to specify location of the symbol on the drawing, identification of the integrated circuit, and card location. The example NAND gate is located on sheet 2 at coordinate D and 4. The integrated circuit reference designator on this circuit card is U2 and the circuit card is the first card in the third row. In some cases a single alphanumeric digit appears designating the card location. Numbers adjacent to the logic symbols within parenthesis identify unique pin numbers on the integrated circuit. Numbers adjacent to the logic symbol which are not within parentheses identify unique circuit card pin numbers.

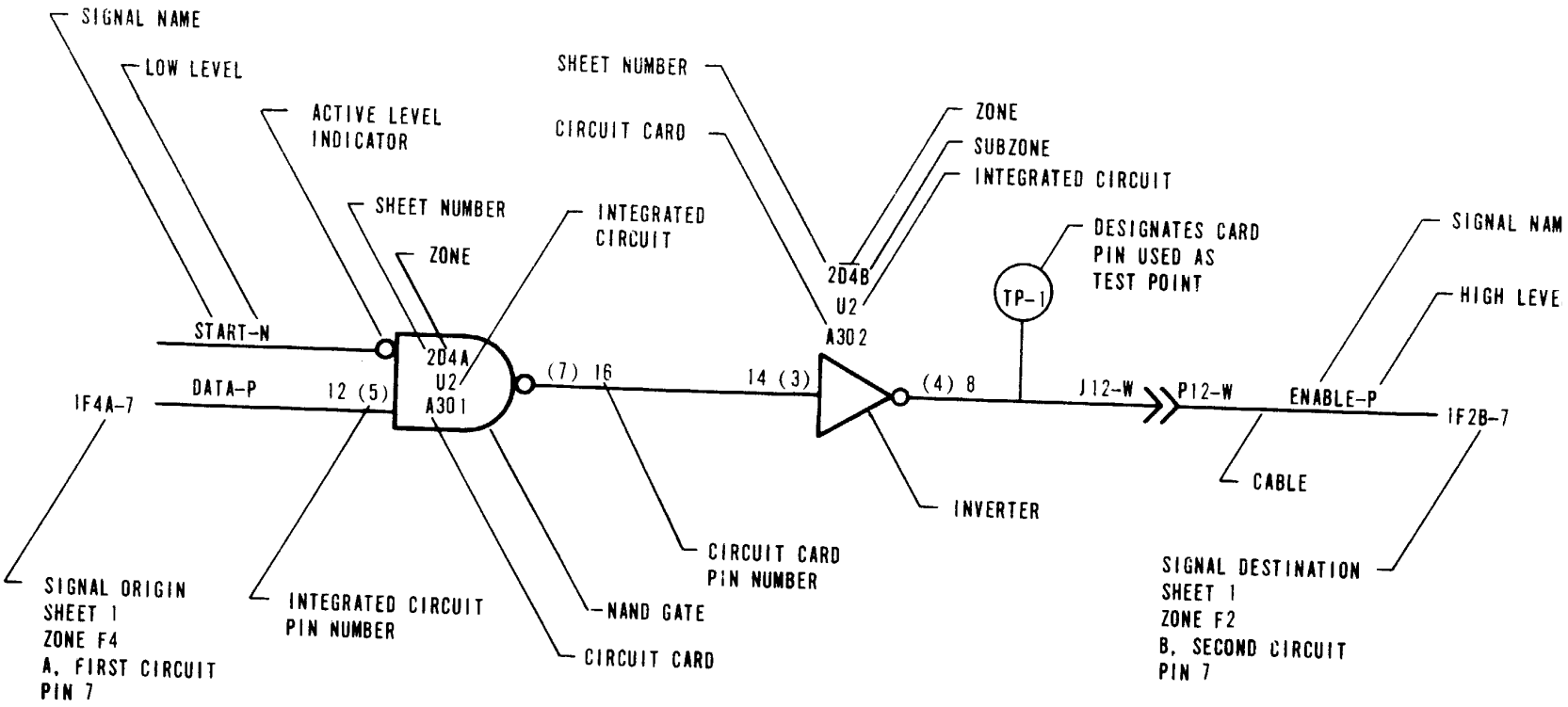

Figure 7-1. Logic Diagram Circuit Labeling

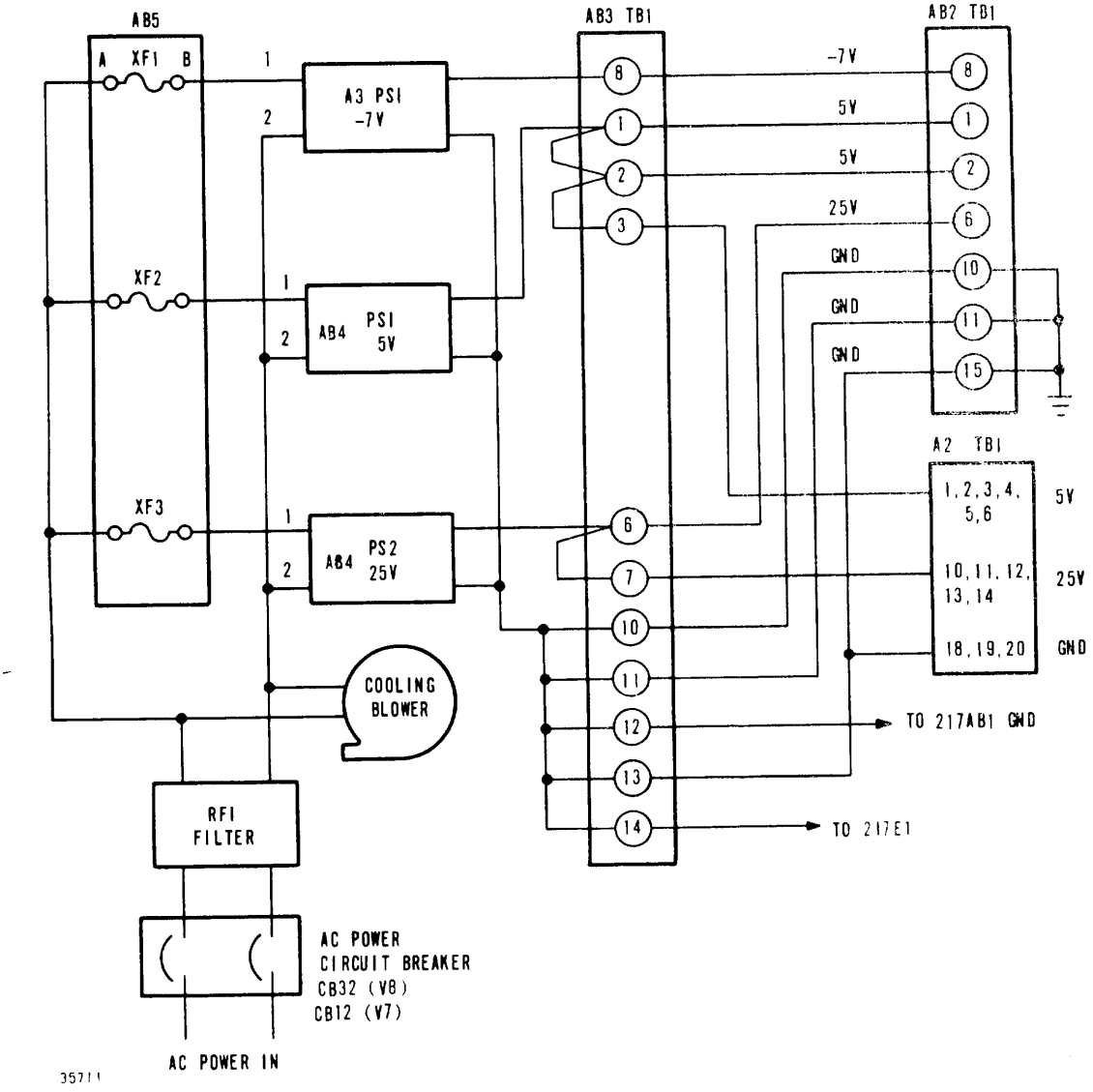

Figure 7-2. Ac, Dc Power distribution, Somc

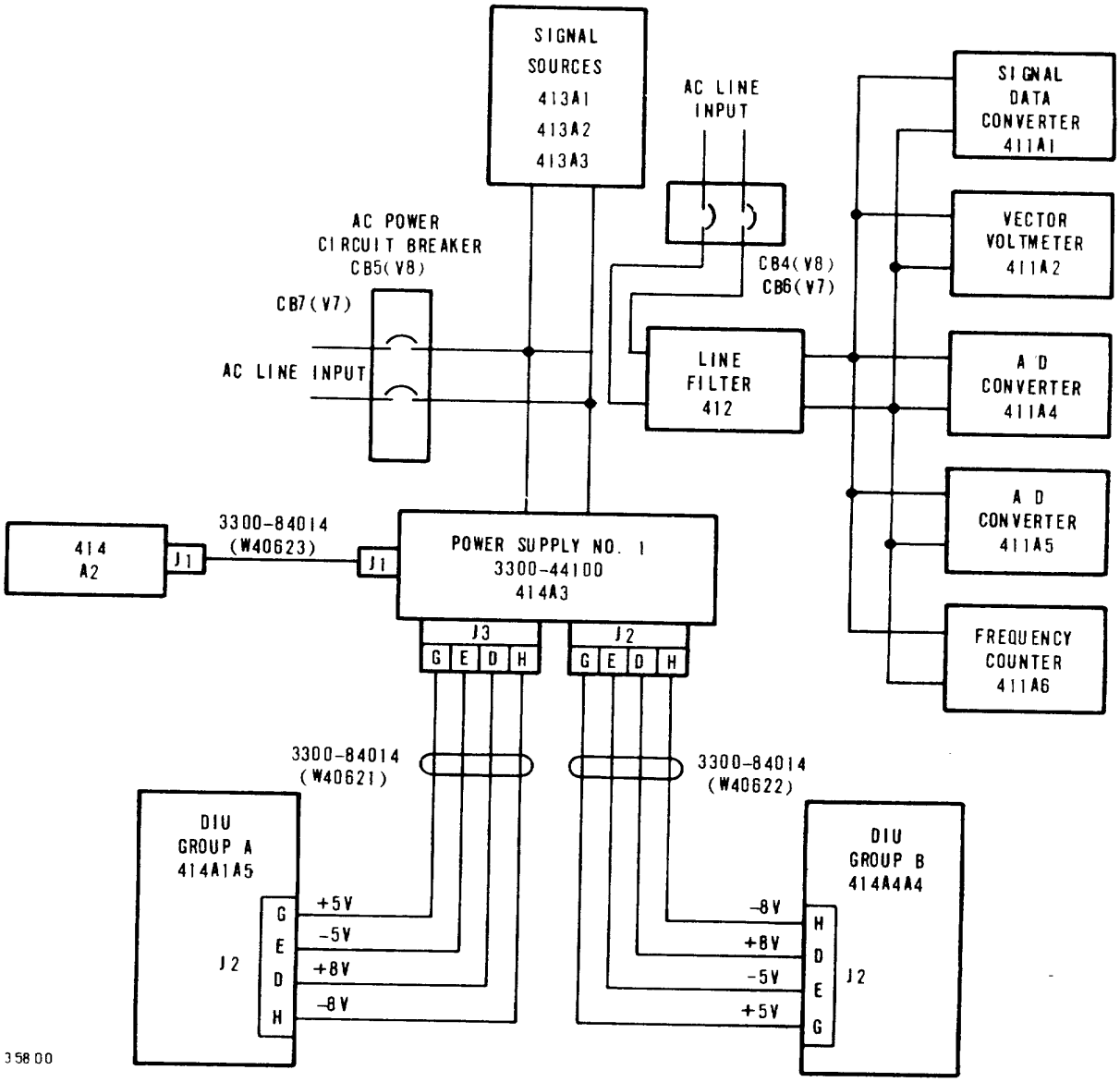

Figure 7-3. Ac, Dc Power Distribution Olm&t, Antenna Building

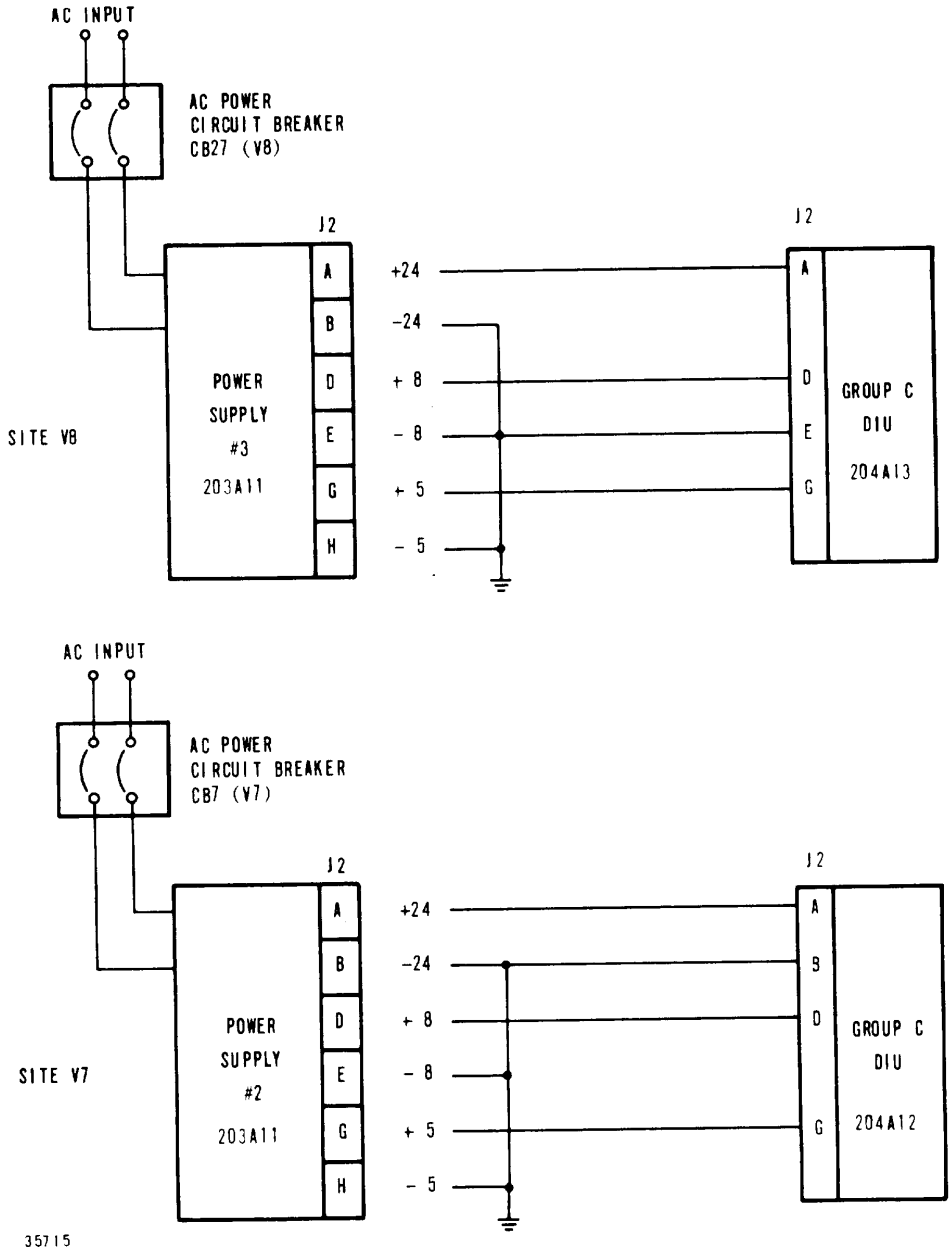

Figure 7-4. Ac, Dc Power distribution to group C Matrix

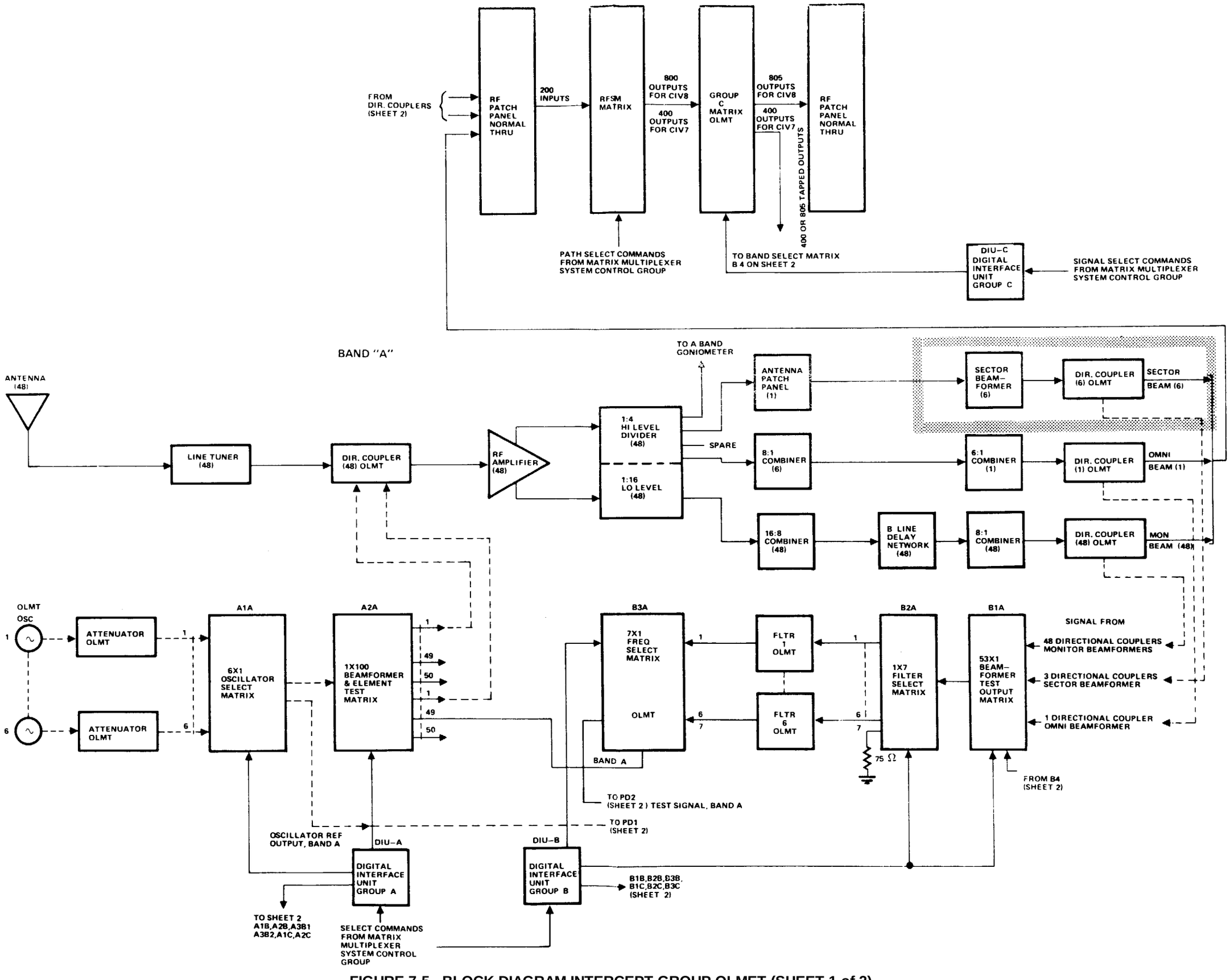

FIGURE 7-5. BLOCK DIAGRAM INTERCEPT GROUP OLMET (SHEET 1 of 2)
CHANGE 1 7-7/7-8

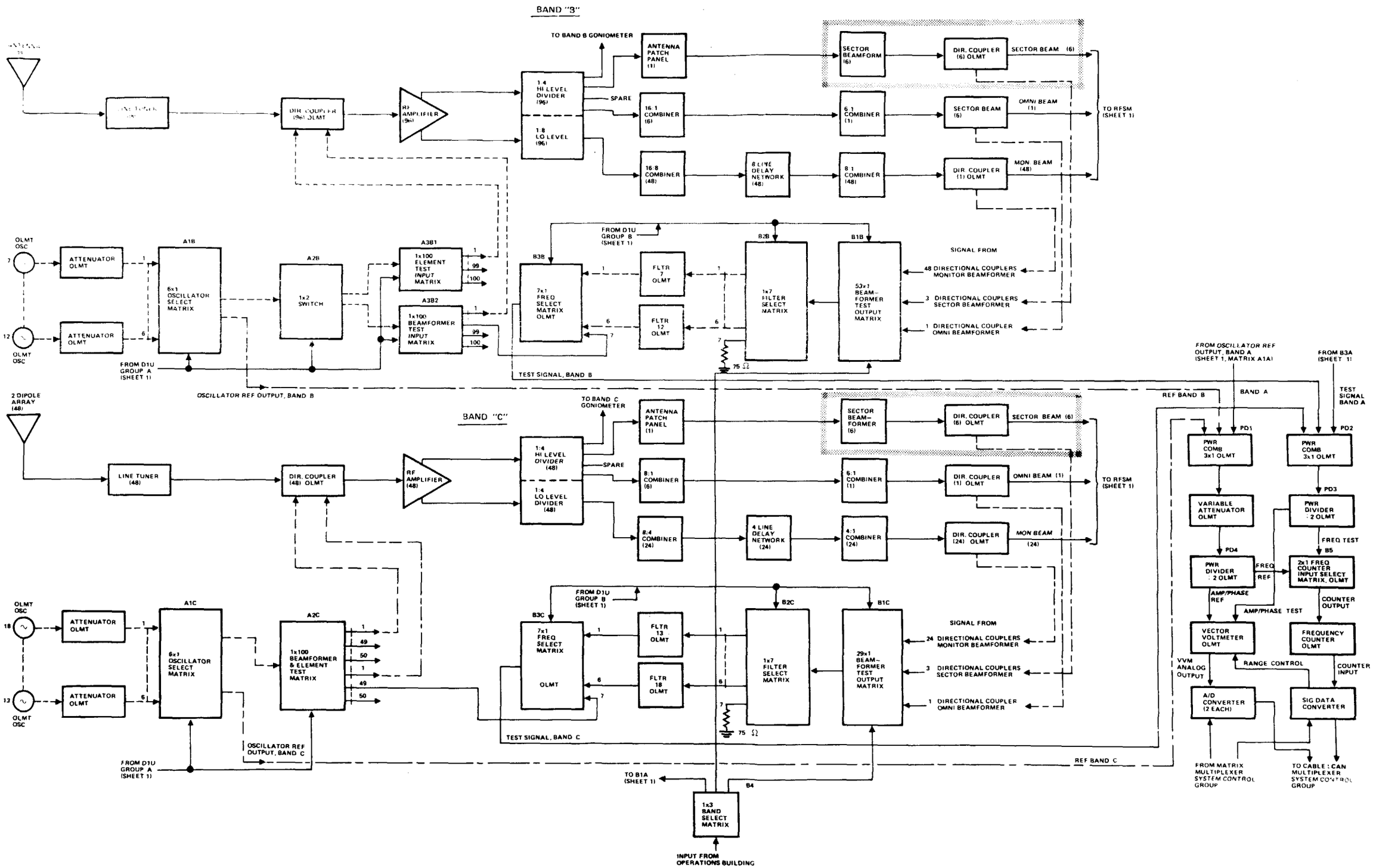

FIGURE 7-5. BLOCK DIAGRAM INTERCEPT GROUP OLM&T (SHEET 2 of 2)
CHANGE 1 7-9/7-10

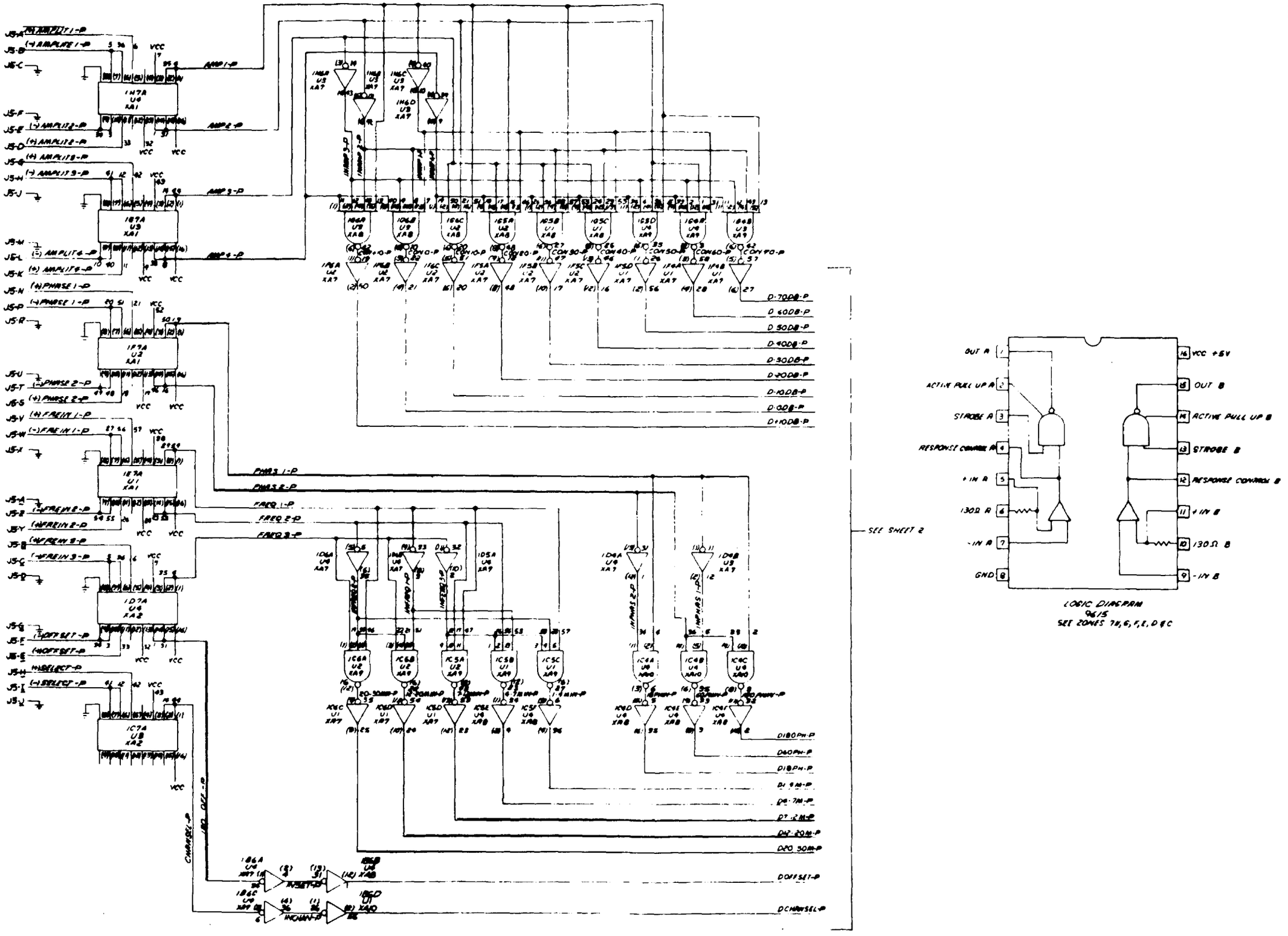

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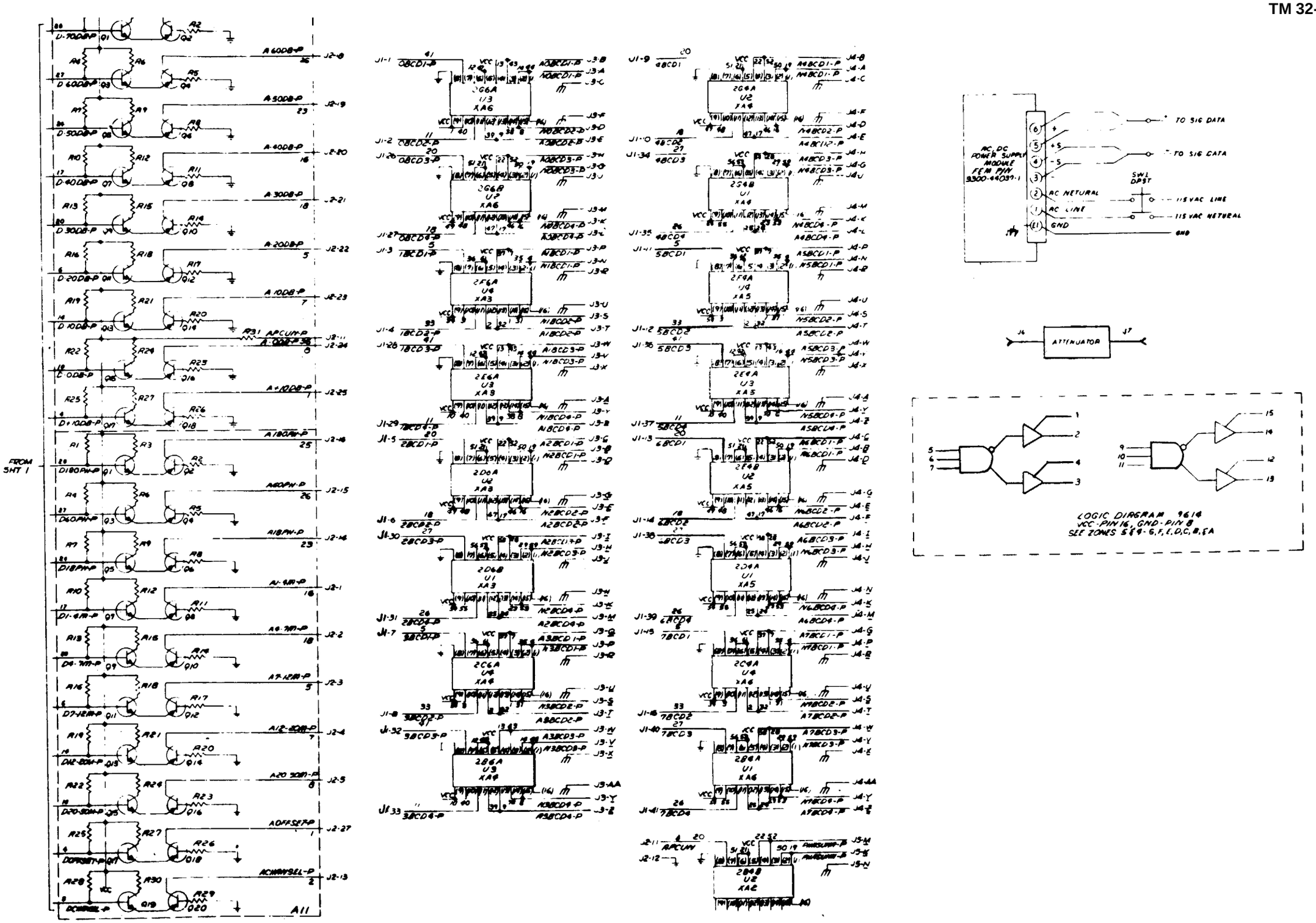
Figure 7-6. System Logic Diagram, Signal Data Converter (Sheet 1 of 2)



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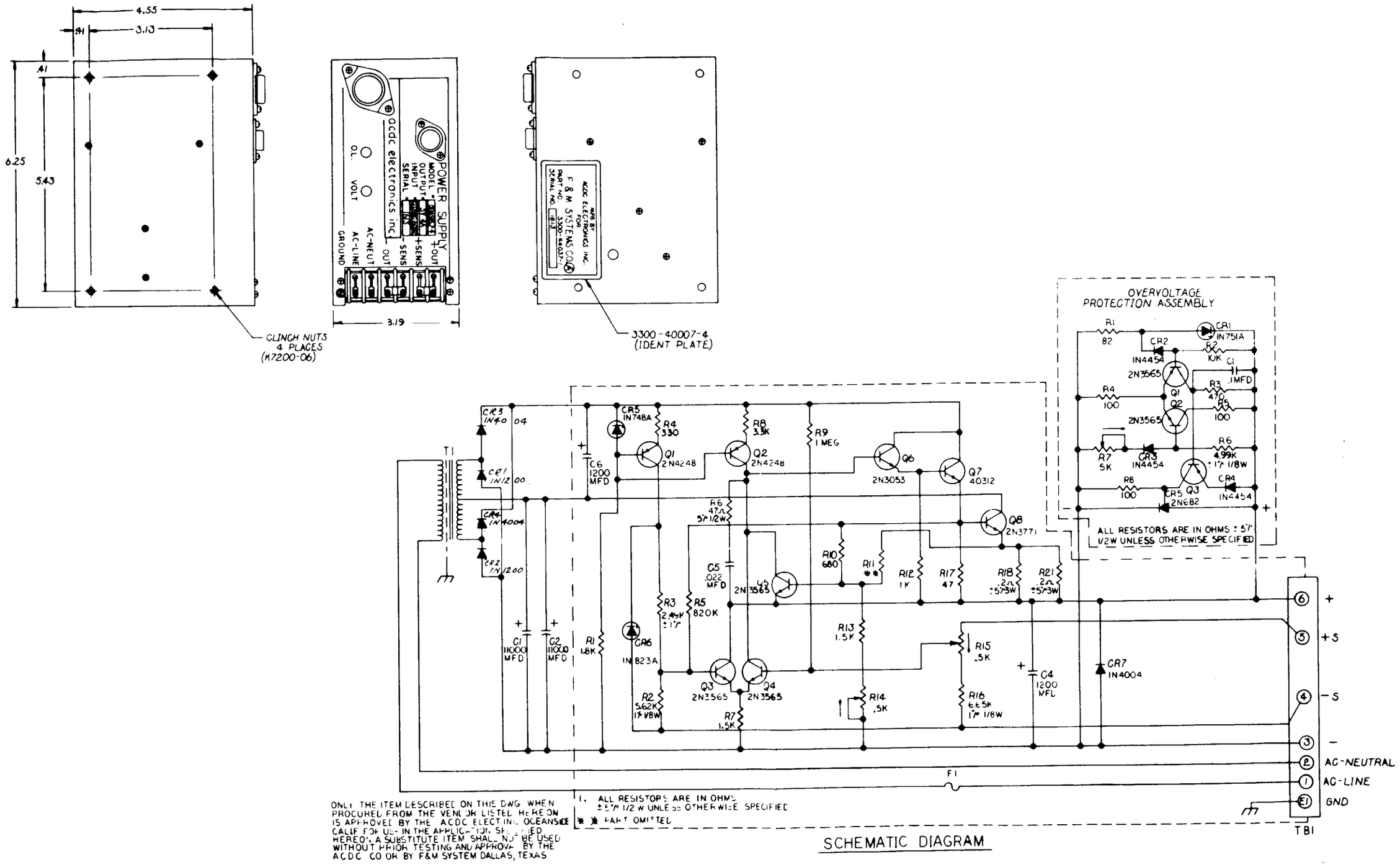
35994

(F&M SYSTEMS CO DRAWING NO 3300-74003,S2) 35994

Figure 7-6. System Logic Diagram, Signal Data Converter (Sheet 2 of 2)



APPROVED SOURCE OF SUPPLY		
VENDOR	VENDOR'S ITEM IDENT NO.	APPLICATION
ACDC ELECT INC OCEANSIDE CALIF.	OEM 5N5 7-4	POWER SUPPLY

(F&M SYSTEMS CO DRAWING NO 3300-44037) 35995

Figure 7-7. Power Supply PP-6813/FLR-9(V) Schematic Diagram

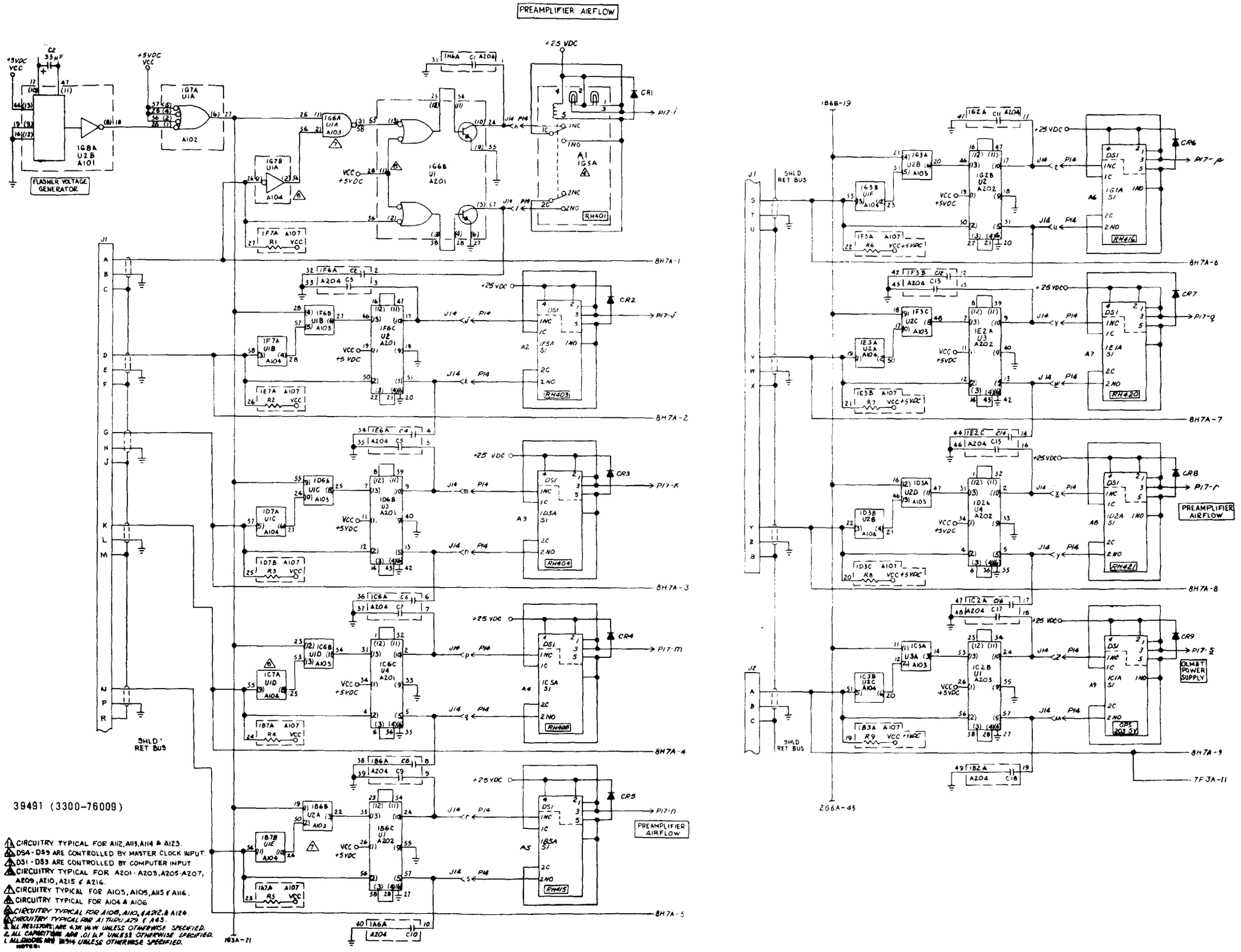


Figure 7-8. Logic Diagram, Somc Controller (Sheet 1 of 11)

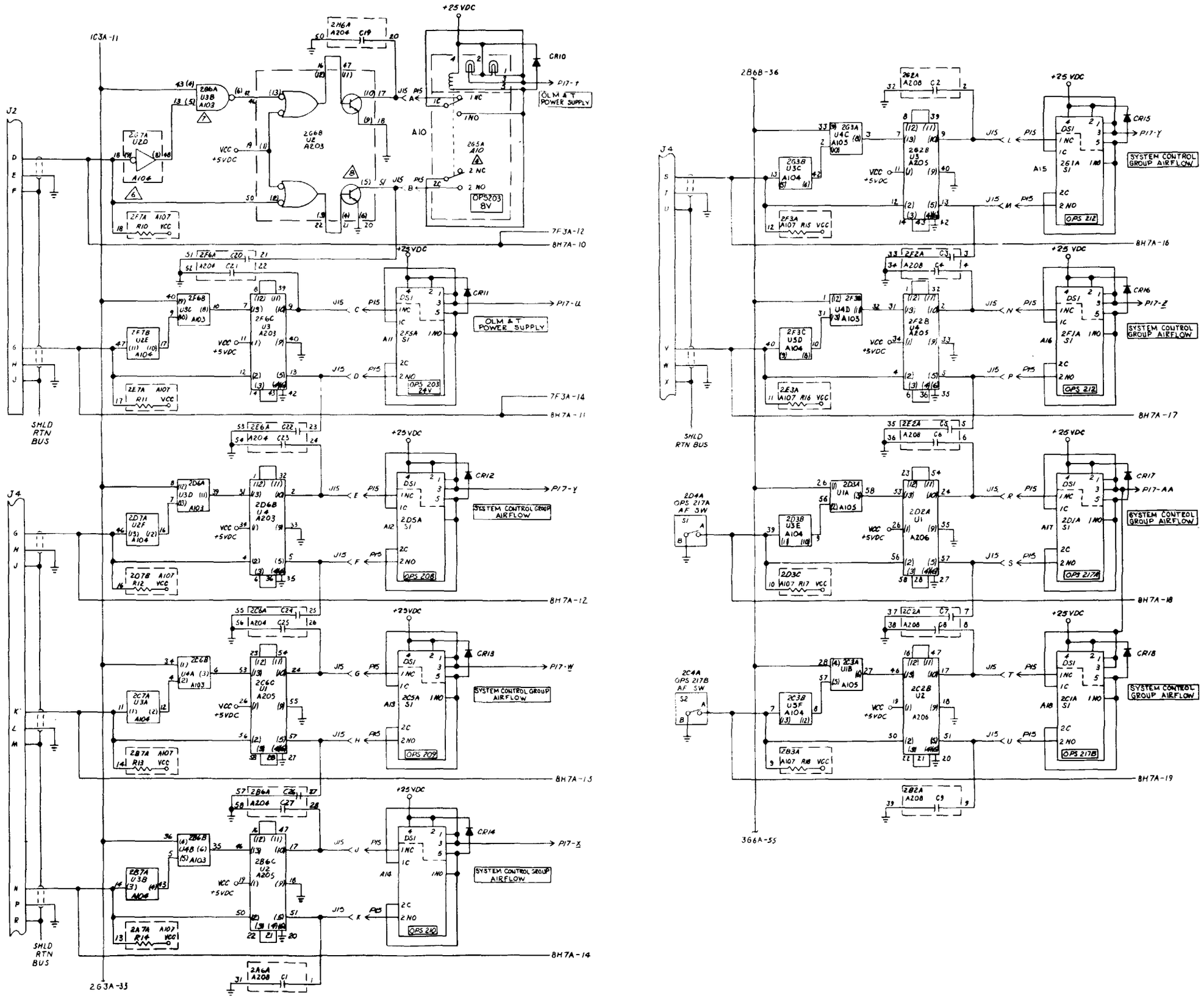
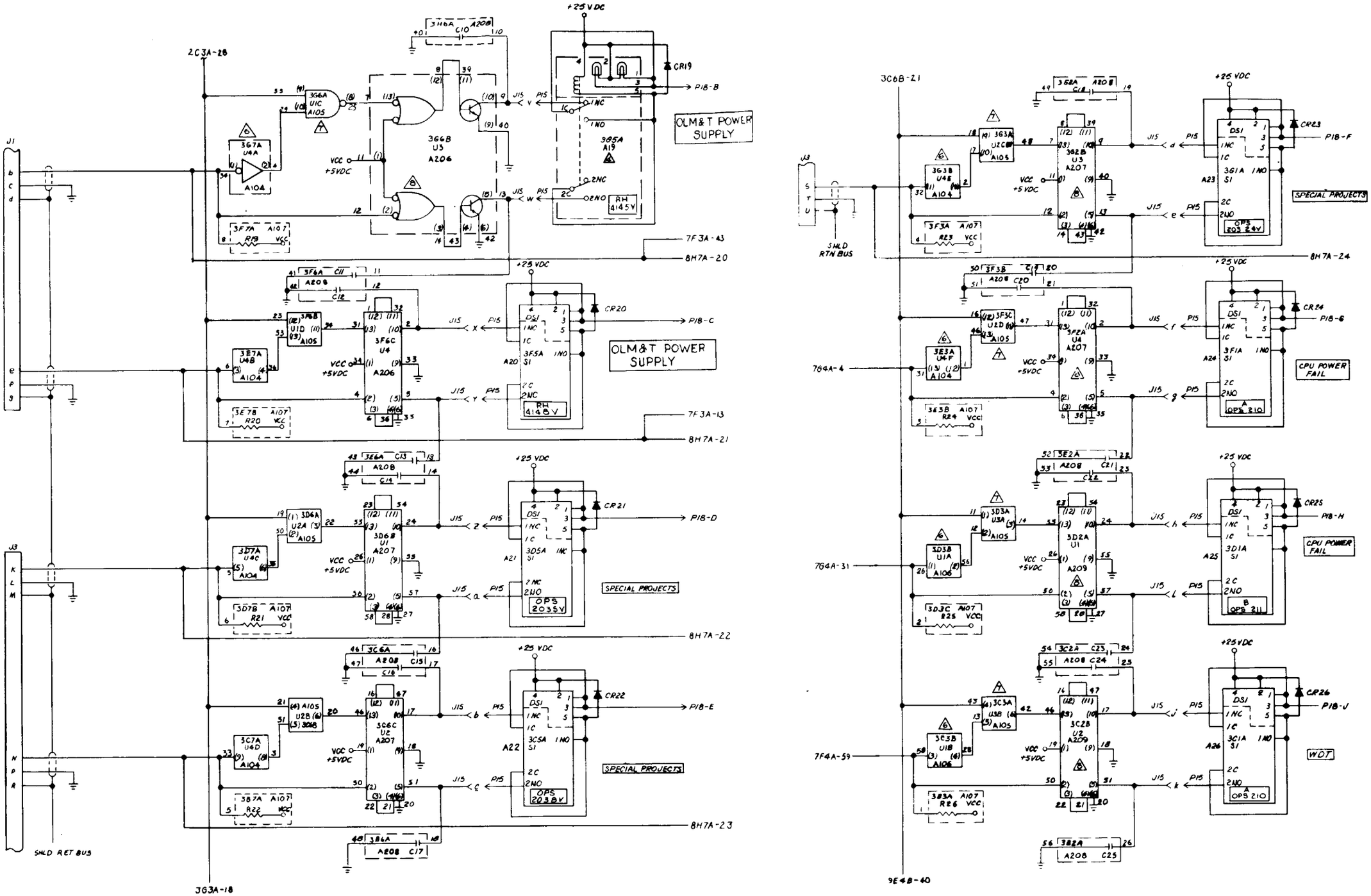


Figure 7-8. Logic Diagram, Somc Controller (Sheet 2 of 11)



39491 (3300-76009)

Figure 7-8. Logic Diagram, Somc Controller (Sheet 3 of 11)

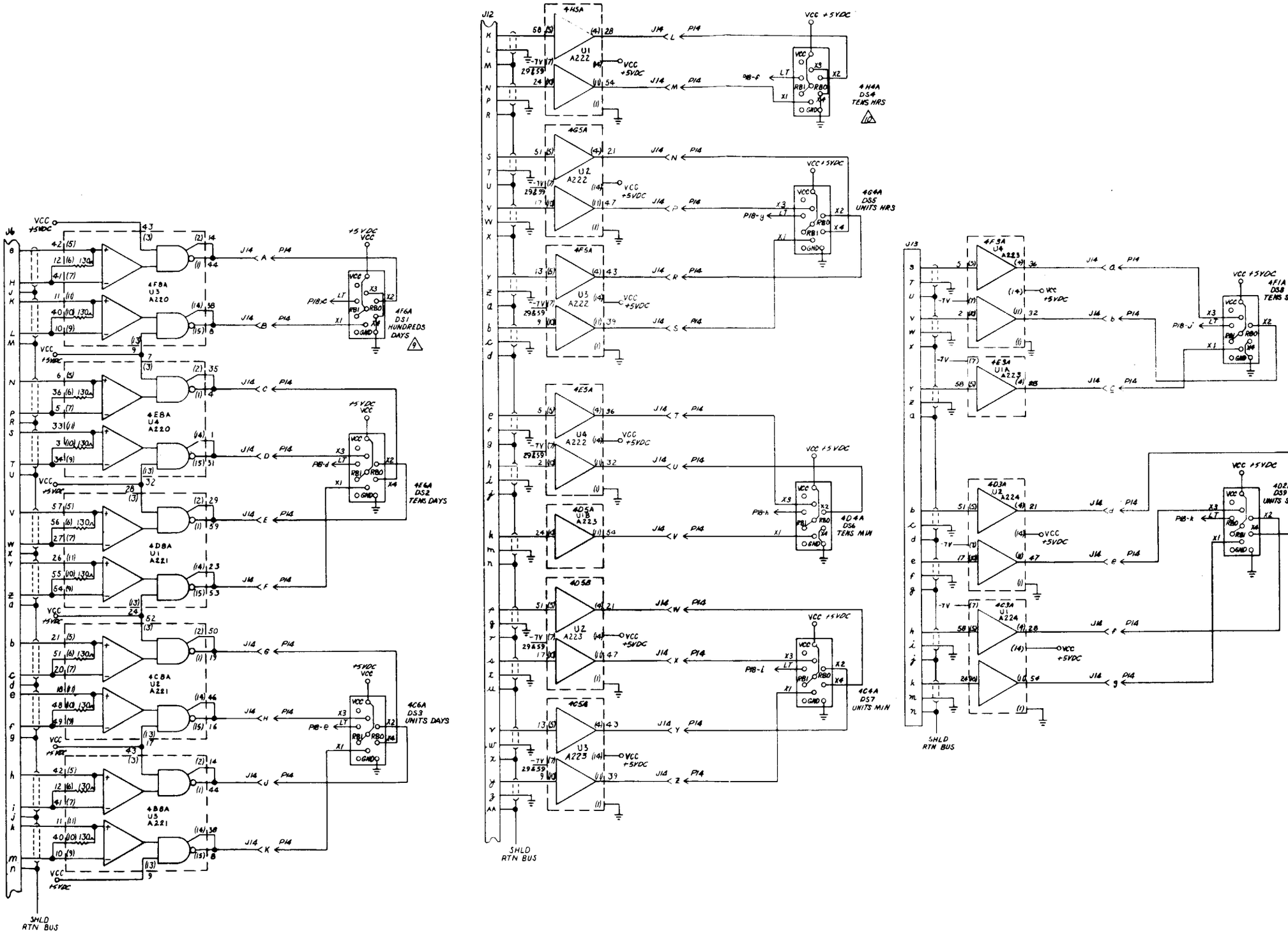


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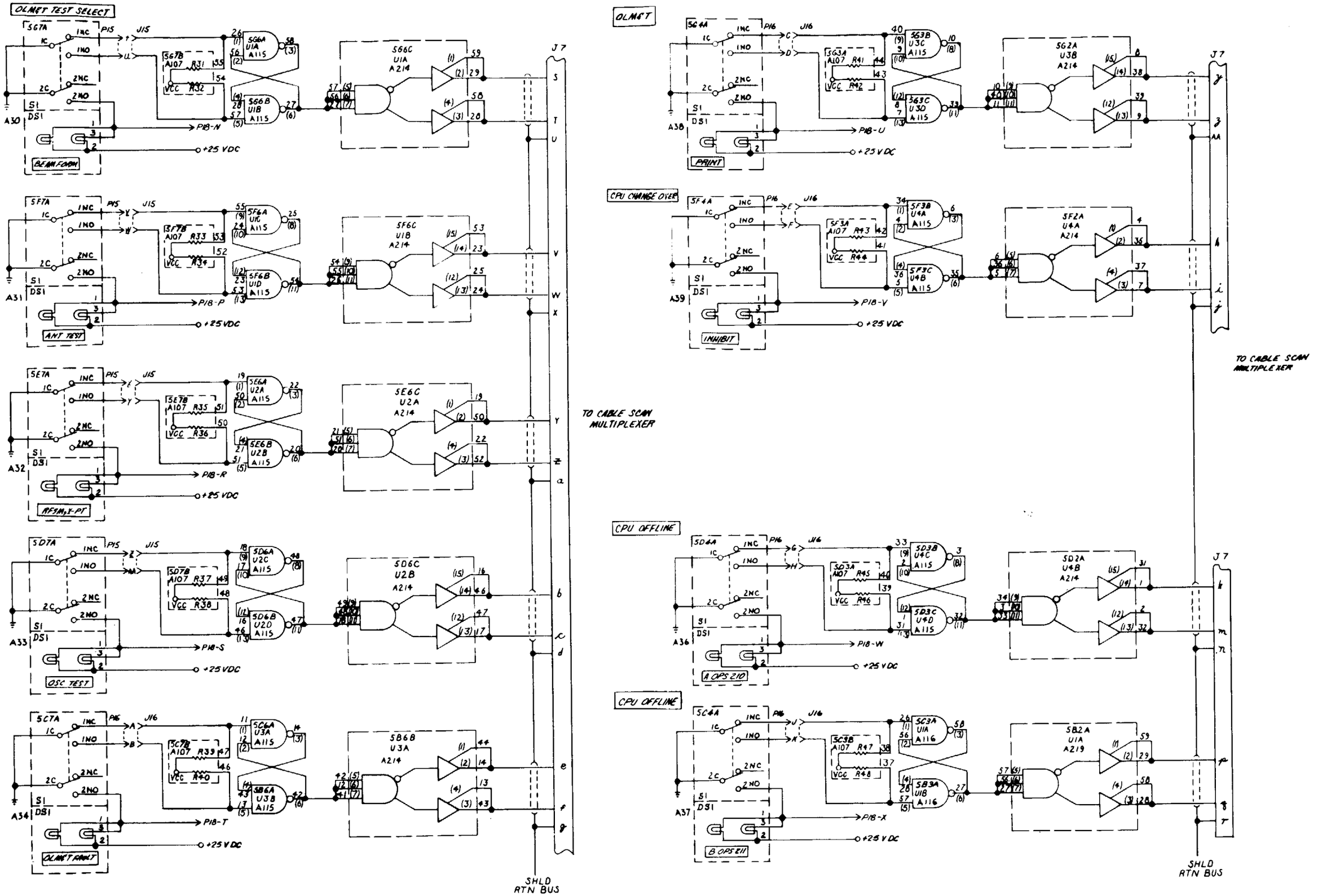
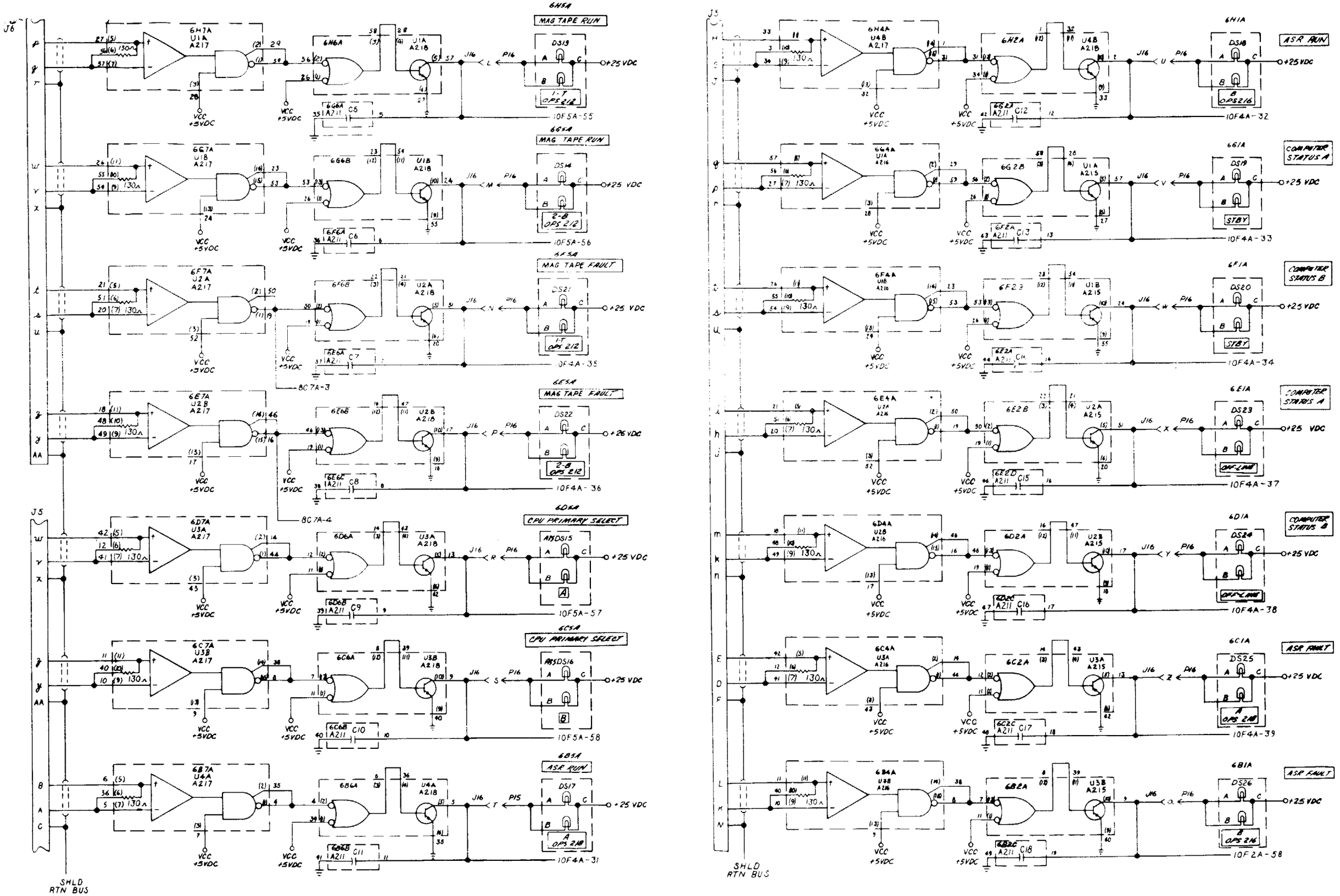
Figure 7-8. Logic Diagram, Somc Controller (Sheet 4 of 11)



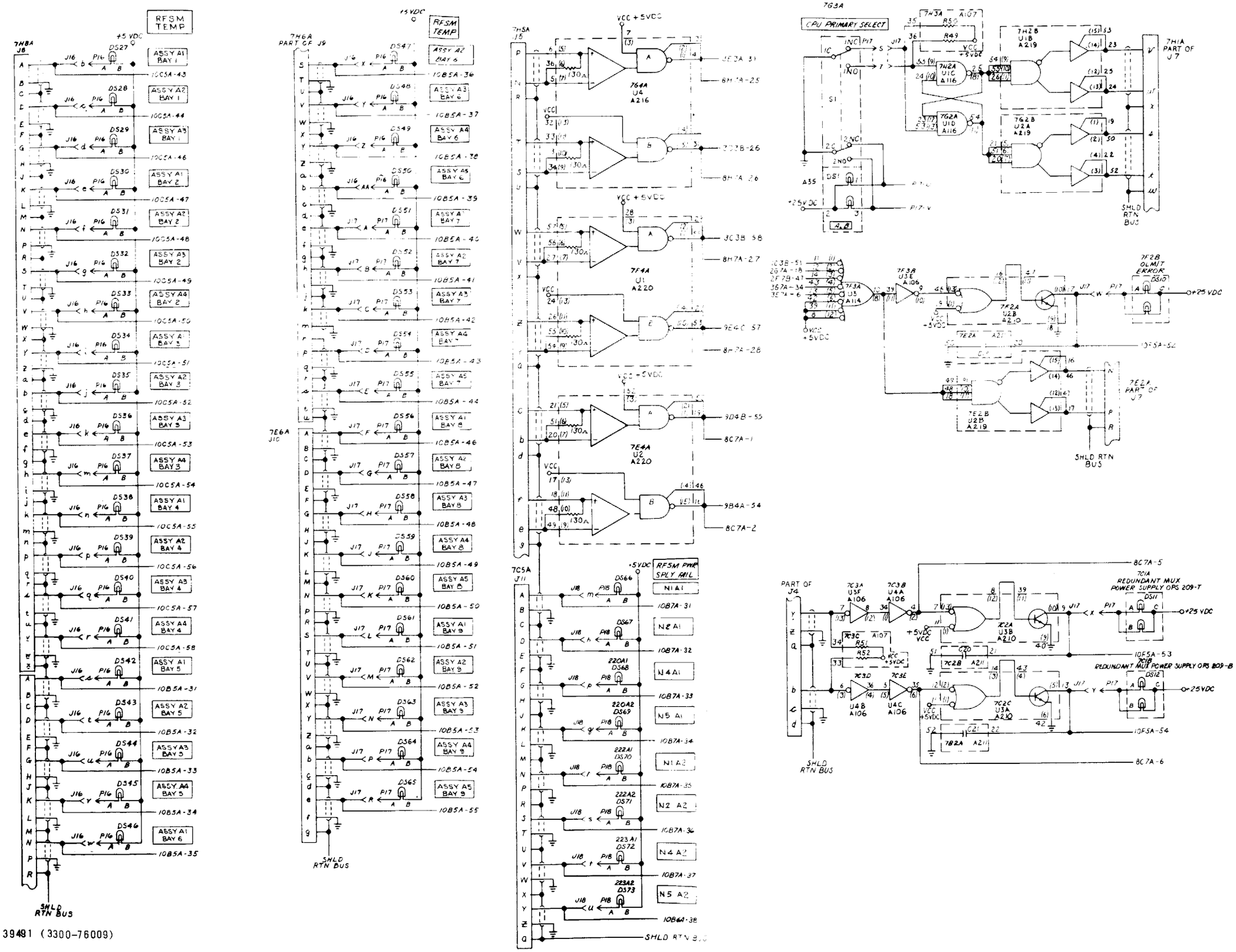
39491 (3300-76009)

Figure 7-8. Logic Diagram, Somc Controller (Sheet 5 of 11)



39491 (3300-76009)

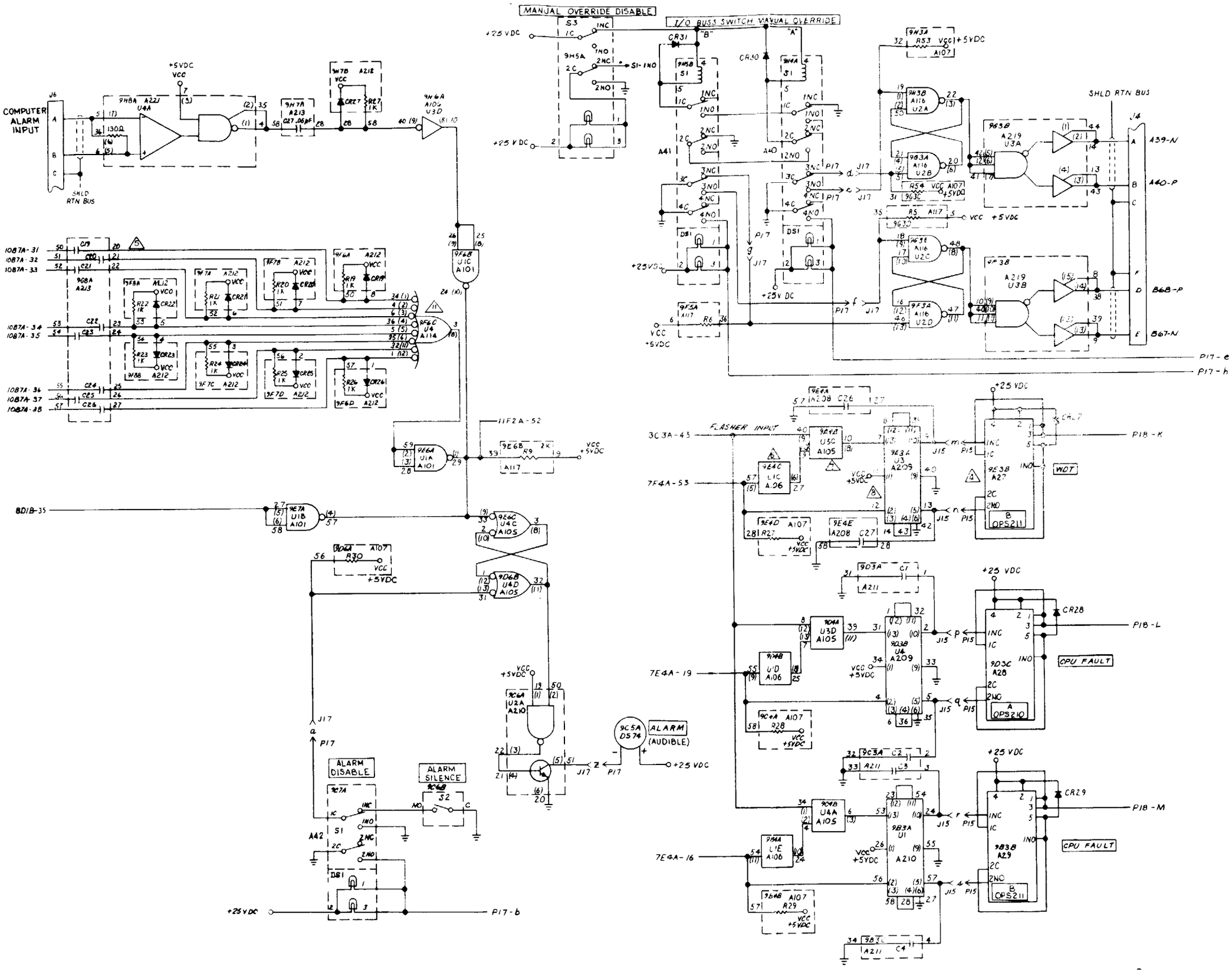
Figure 7-8. Logic Diagram, Somc Controller (Sheet 6 of 11)



39491 (3300-76009)

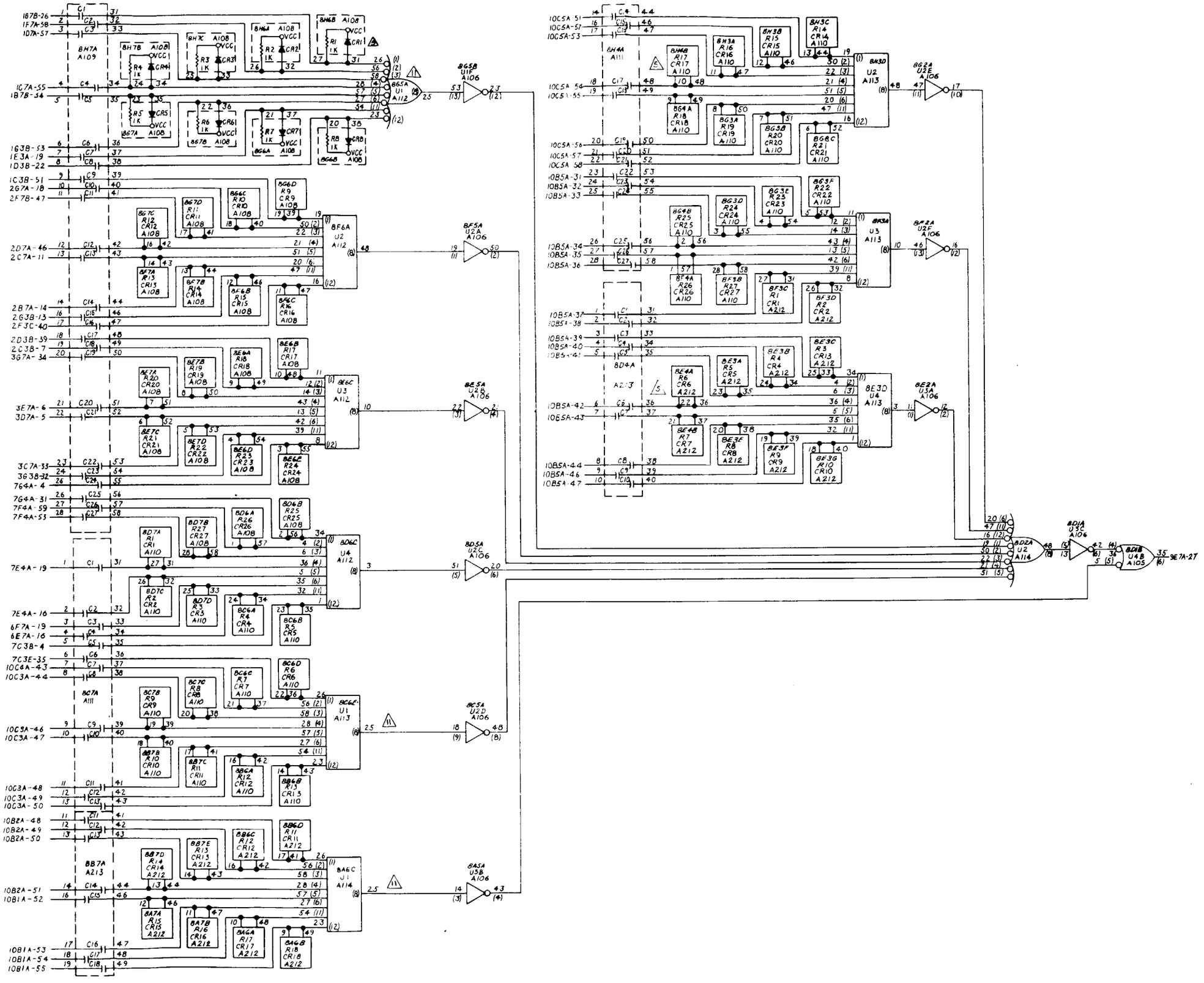
39491 (3300-76009)

Figure 7-8. Logic Diagram, Somc Controller (Sheet 7 of 11)



39491 (3300-76009)

Figure 7-8. Logic Diagram, Somc Controller (Sheet 9 of 11)



39491 (3300-76009)

Figure 7-8. Logic Diagram, Somc Controller (Sheet 8 of 11)

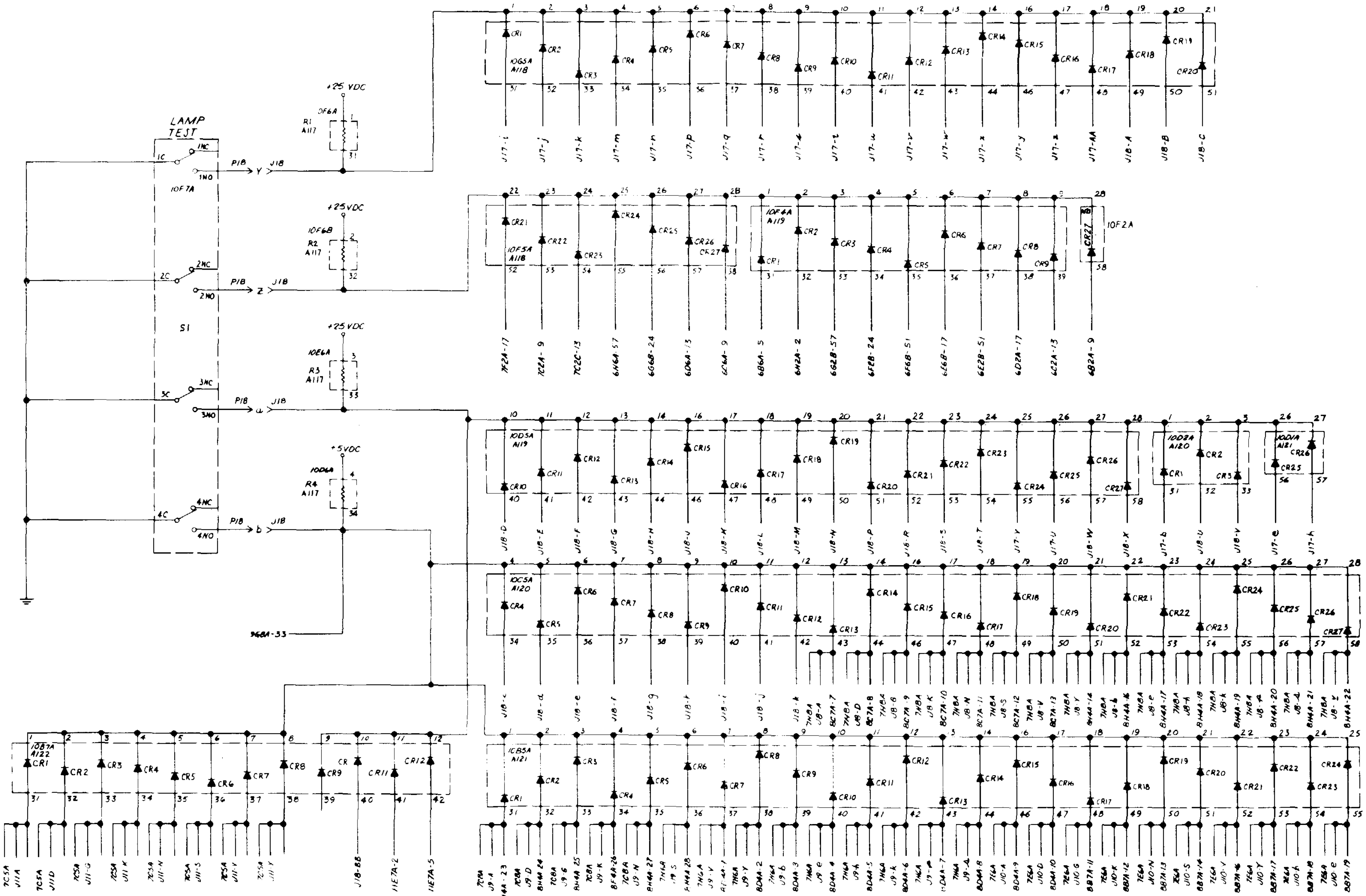


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Figure 7-8. Logic Diagram, Somc Controller (Sheet 10 of 11)

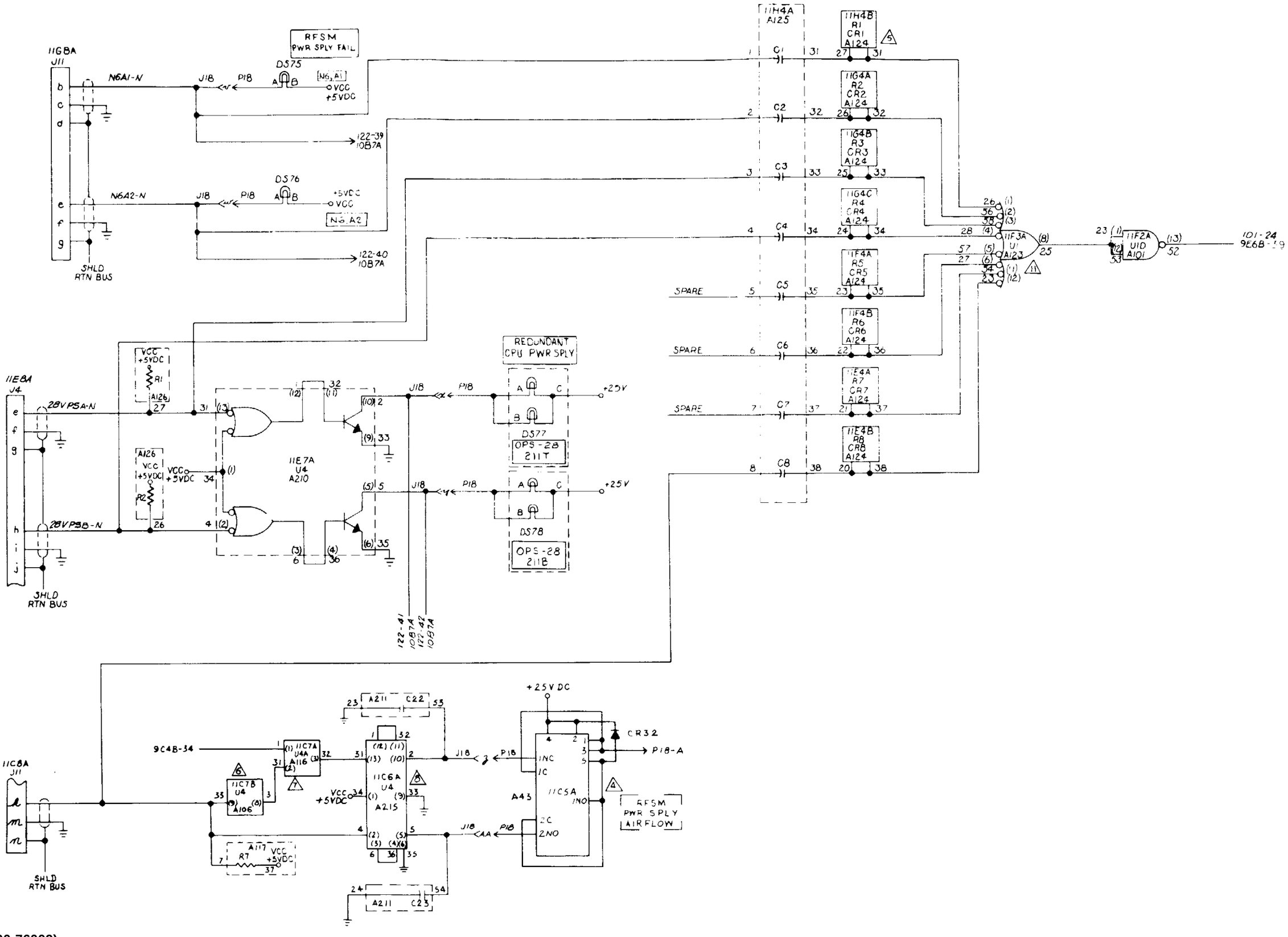

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Figure 7-8. Logic Diagram, Somc Controller (Sheet 11 of 11)

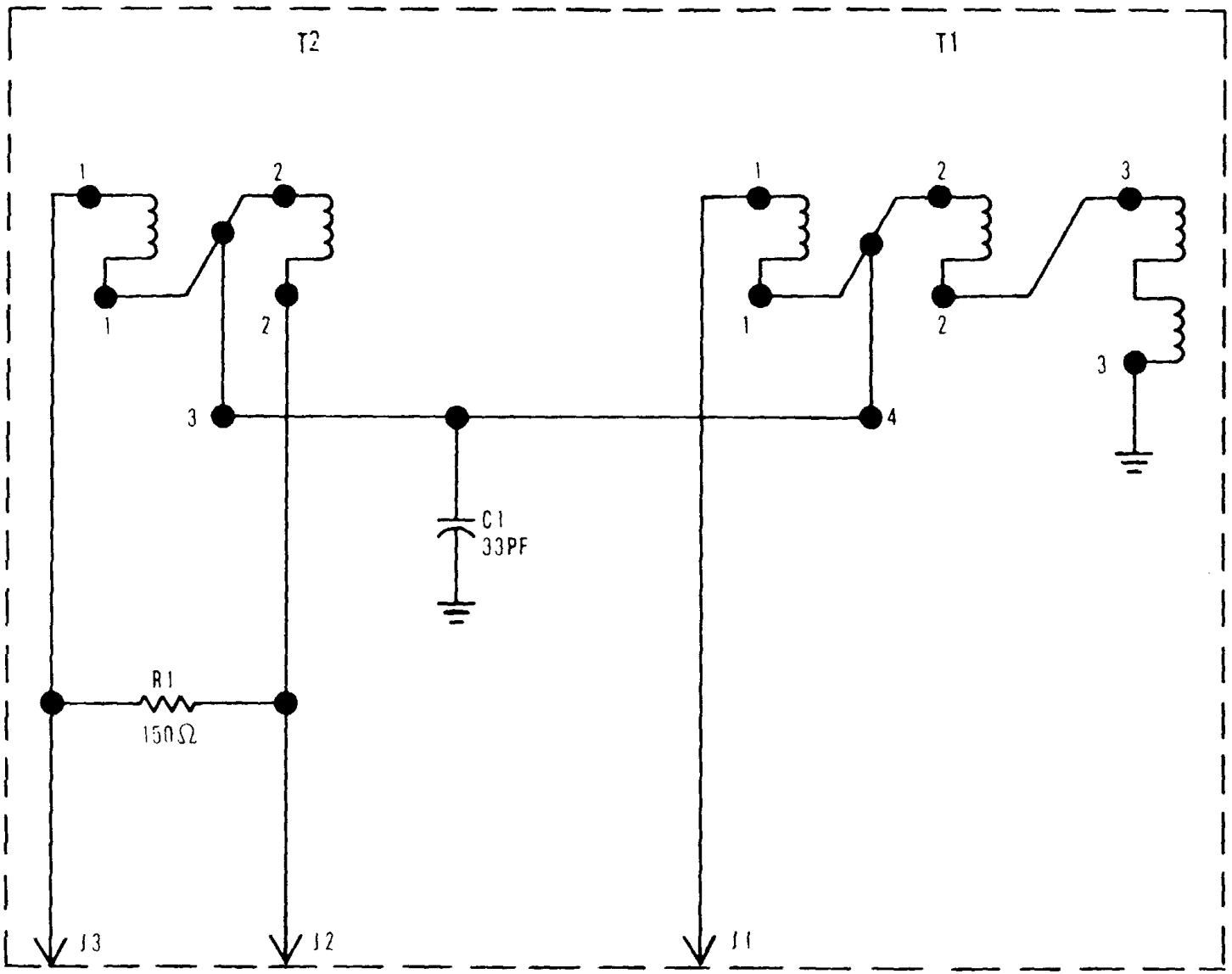

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Figure 7-9. Schematic Diagram, Two-Way Power Divider

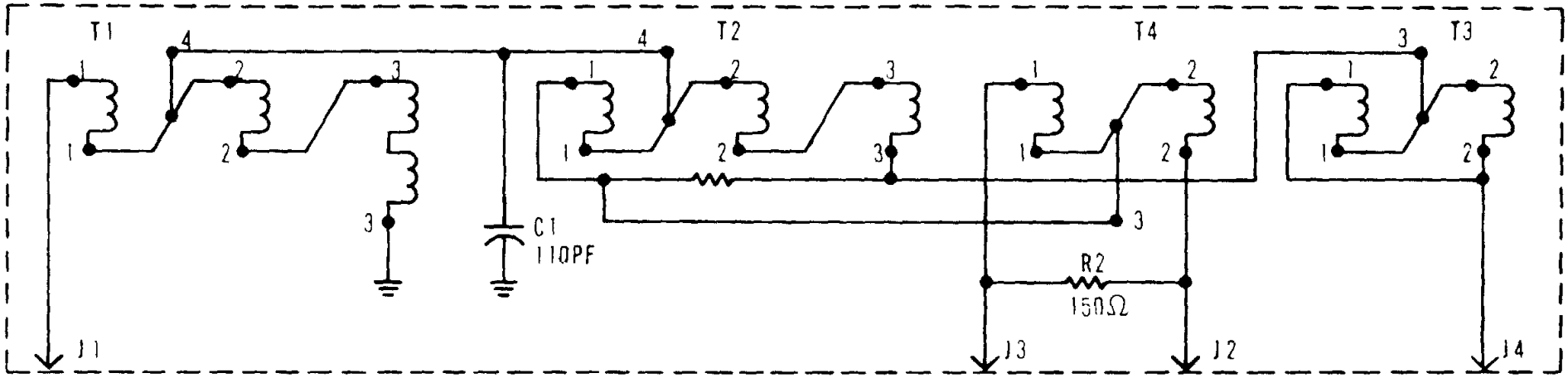

Figure 7-10. Schematic Diagram, Three-Way Power Divider

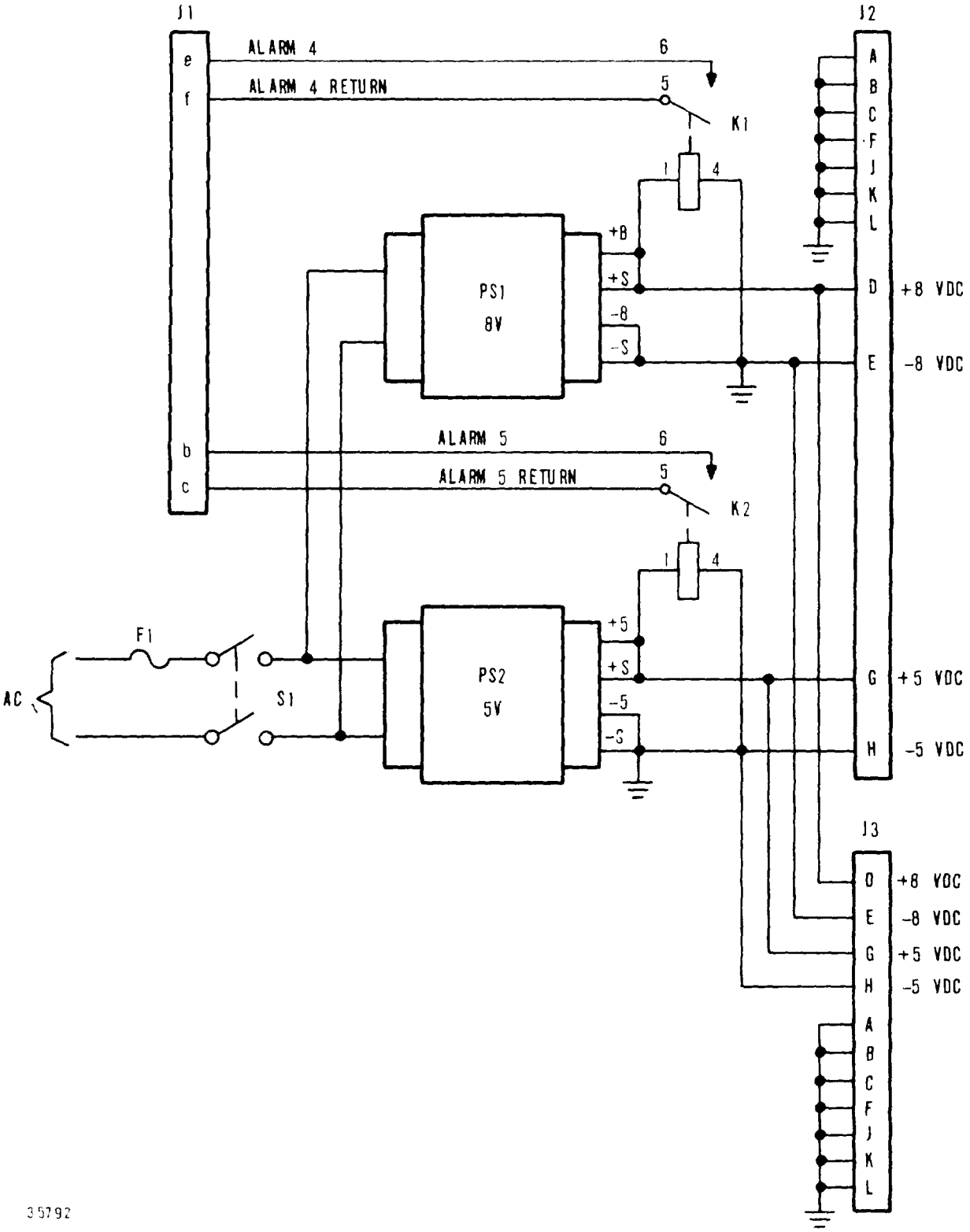

Figure 7-11. Schematic Diagram, Power Supply PP-6811/FLR-9(V) (Power Supply No. 1)(V7)(V8)

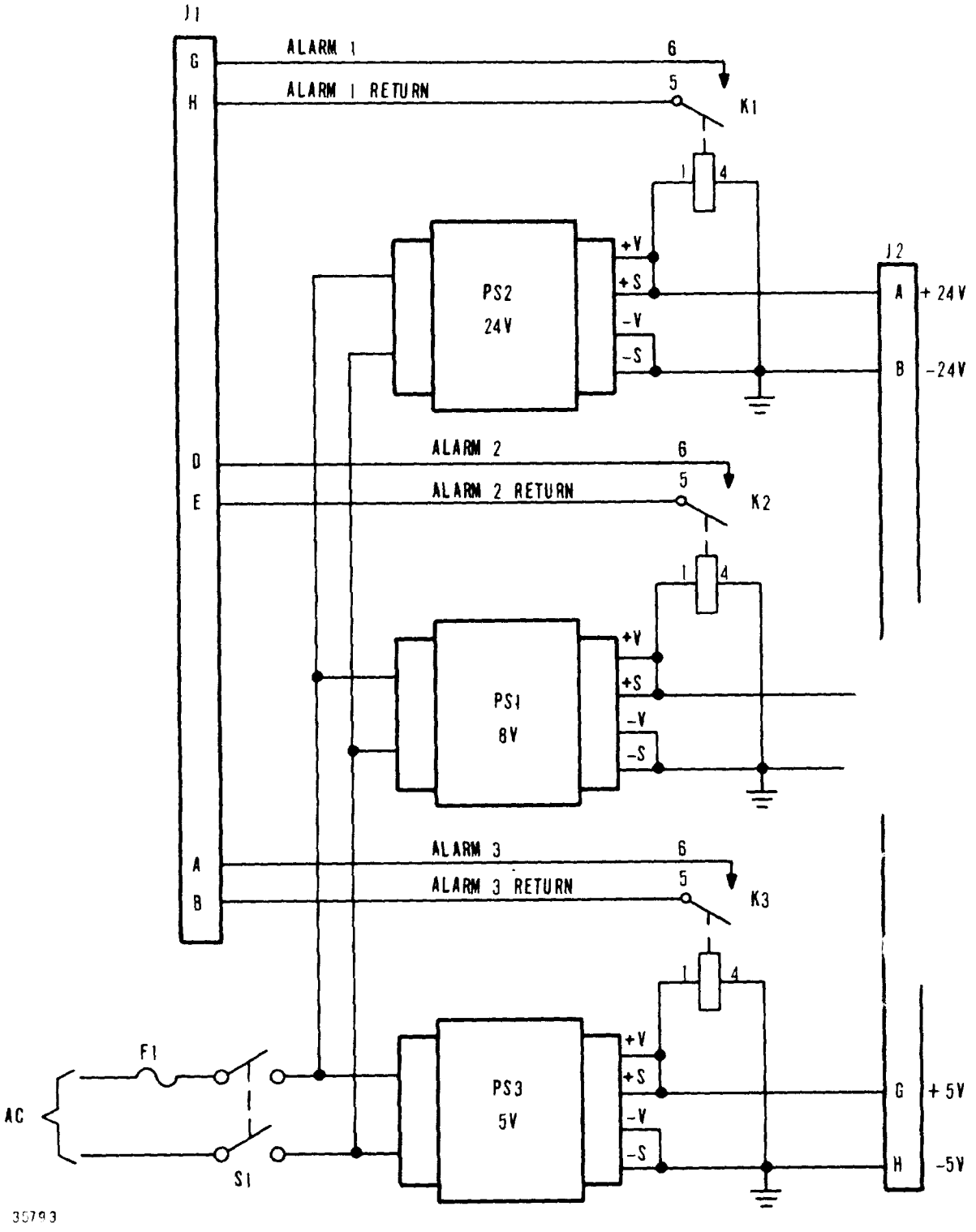

Figure 7-12. Schematic Diagram, Power Supply PP-6810/FLR-9(V) (Power Supply No. 2) (V7)

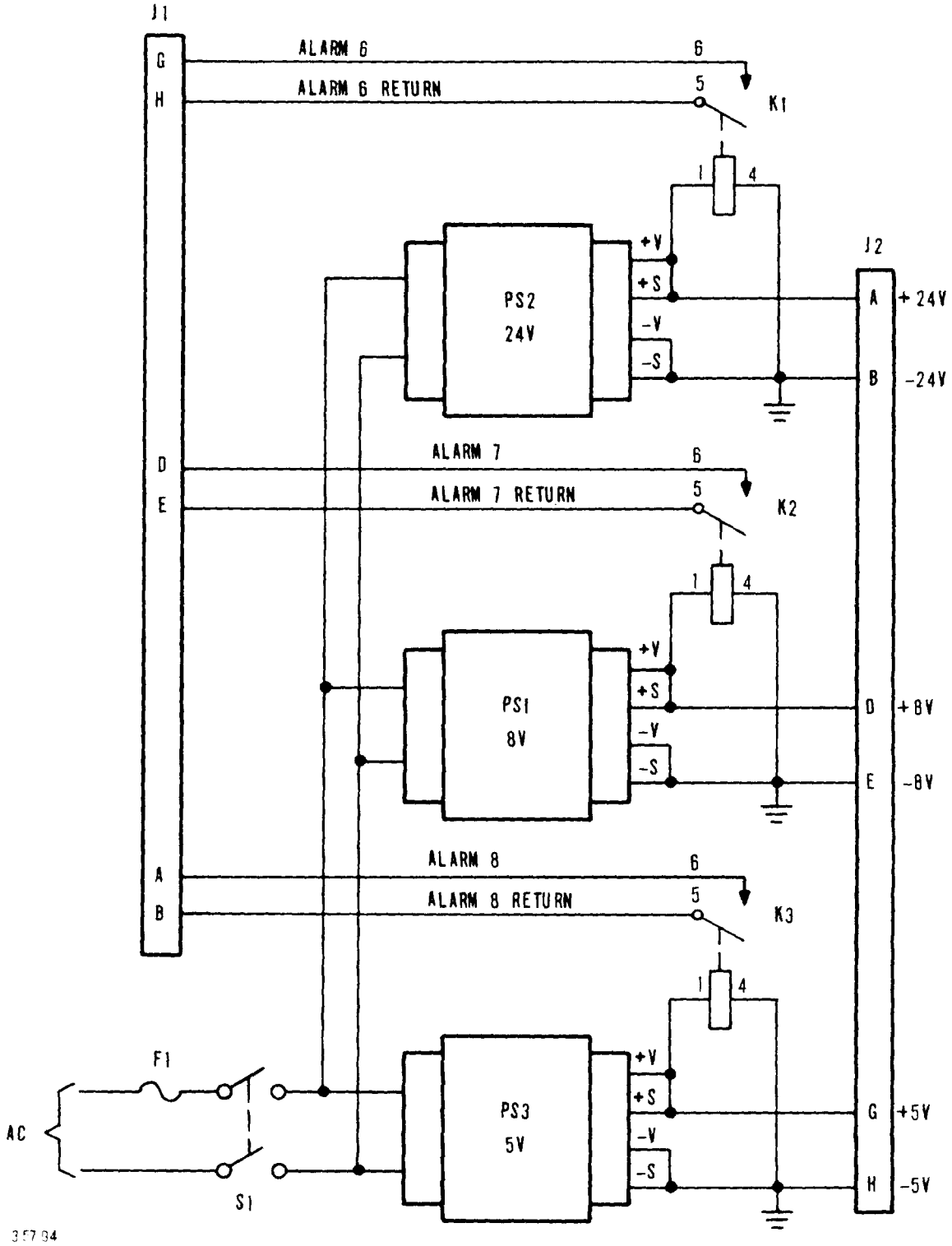

Figure 7-13. Schematic Diagram, Power Supply PP-6814/FLR-9(V) (Power Supply No. 3) (V8)

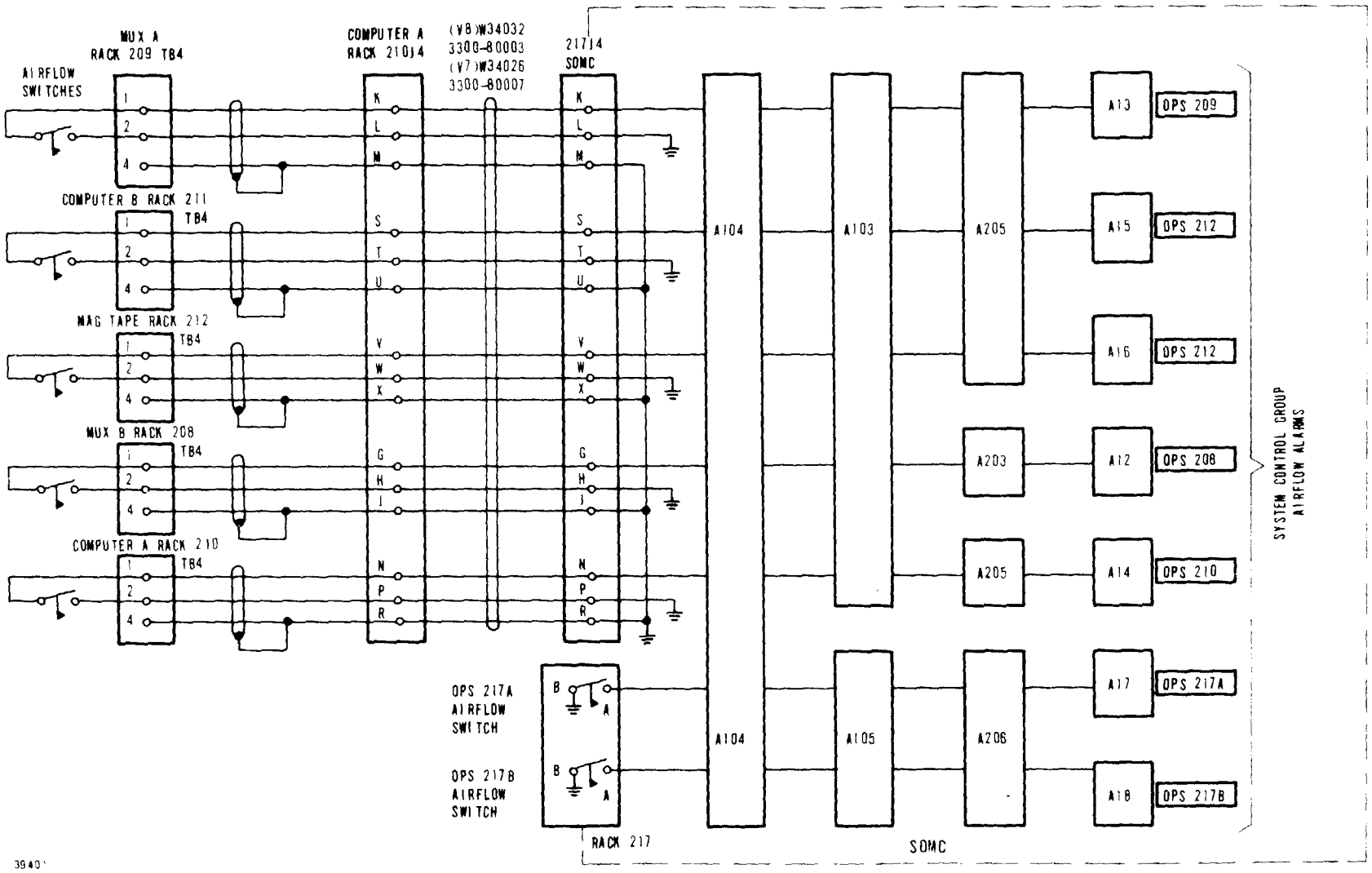

Figure 7-14. Diagram, Airflow Alarms to Somc from System Control Group (V7)(V8)

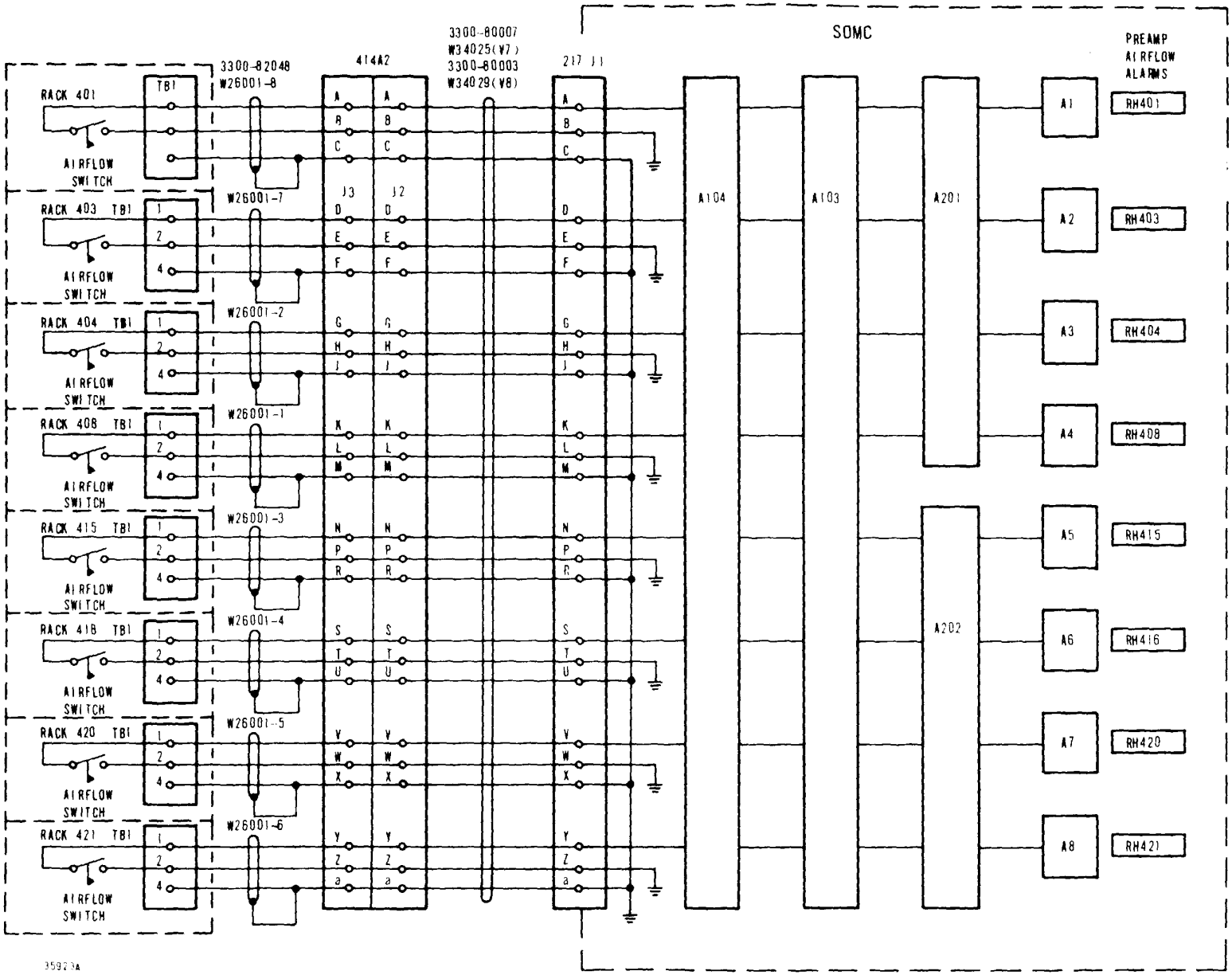

Figure 7-15. Diagram, Airflow Alarms to Somc, Antenna Group (V7)(V8)

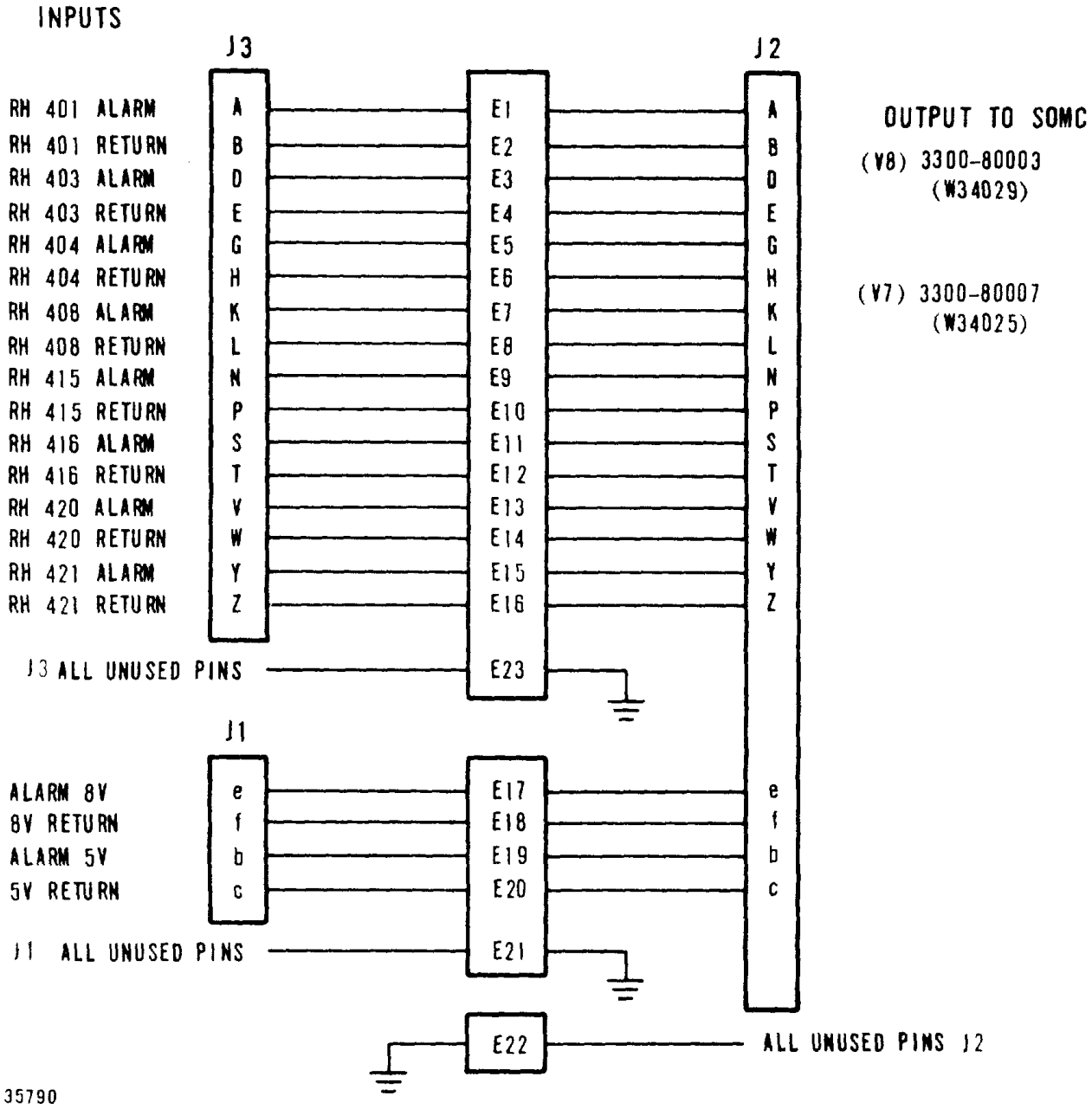

Figure 7-16. Diagram, Alarm Junction Box, 414A2

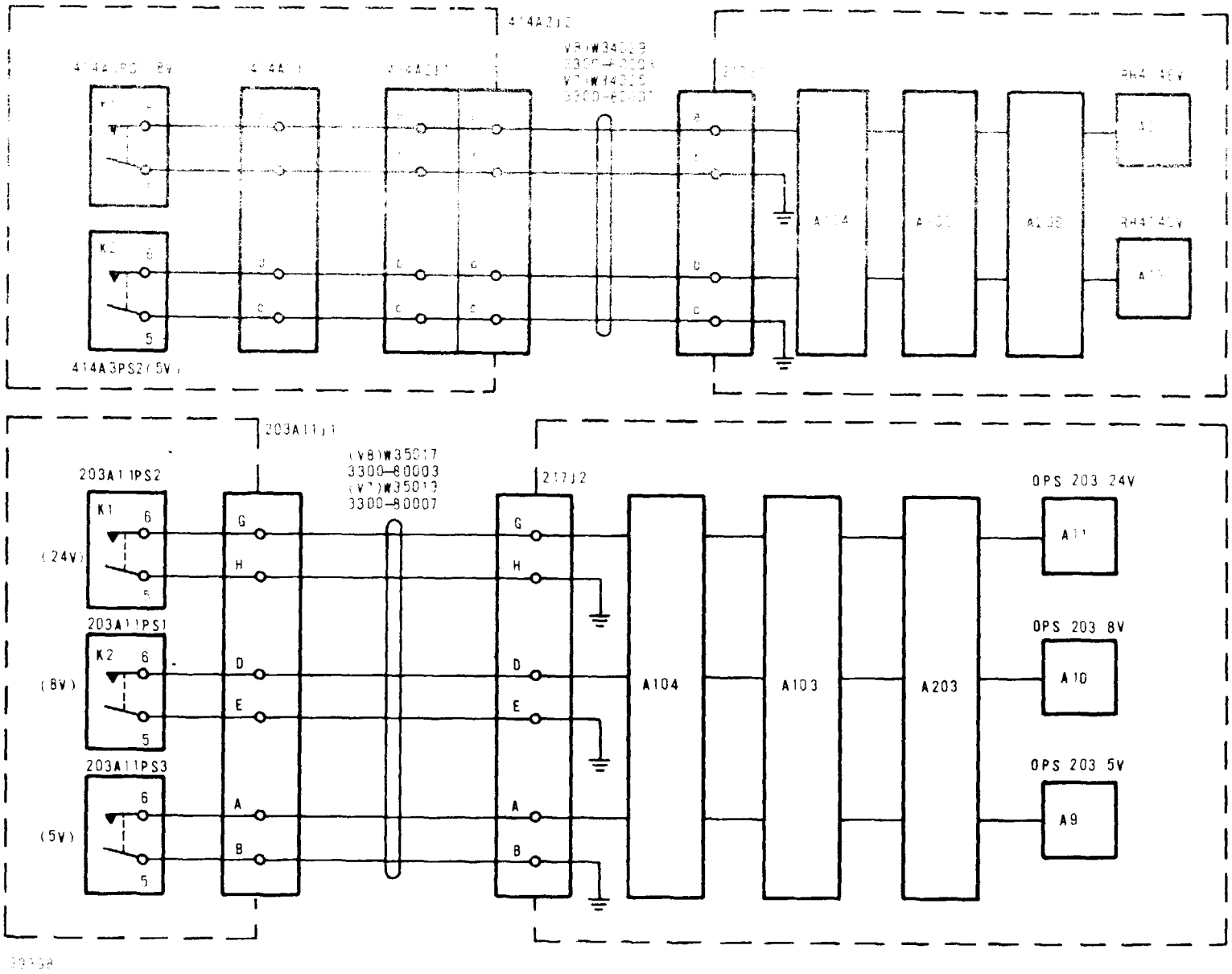

Figure 7-17. Diagram, Olm&t Power Supply Alarms (V7)(V8)

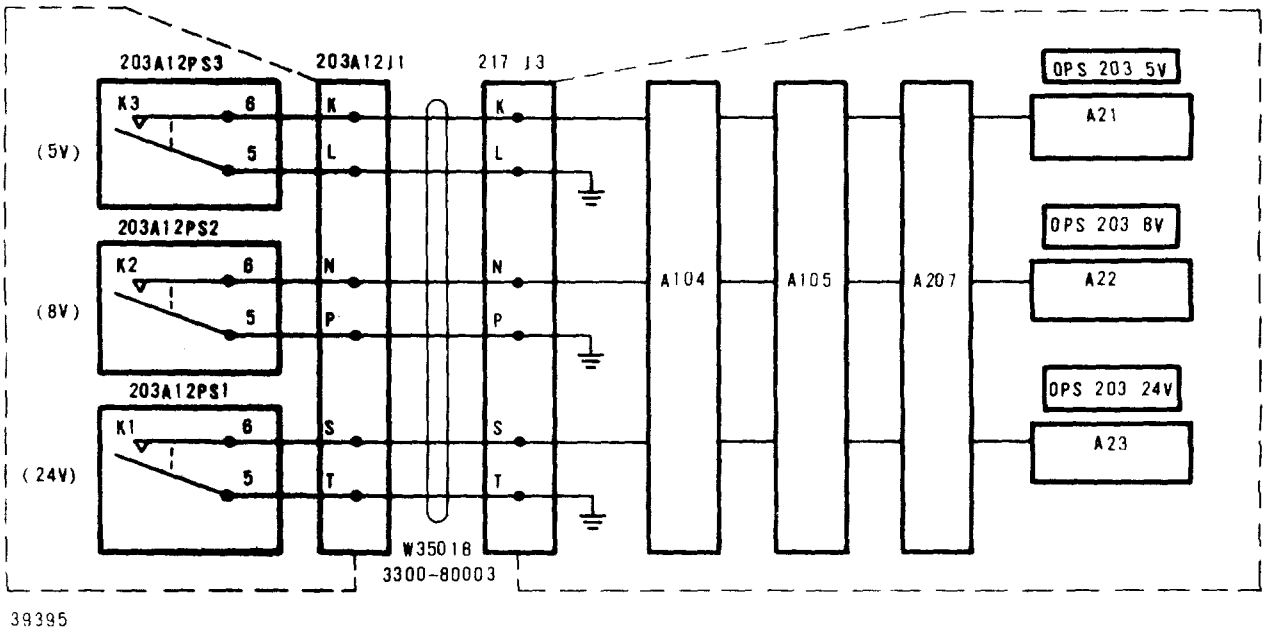

Figure 7-18. Diagram, Special Projects Power Supply Alarms (V8)

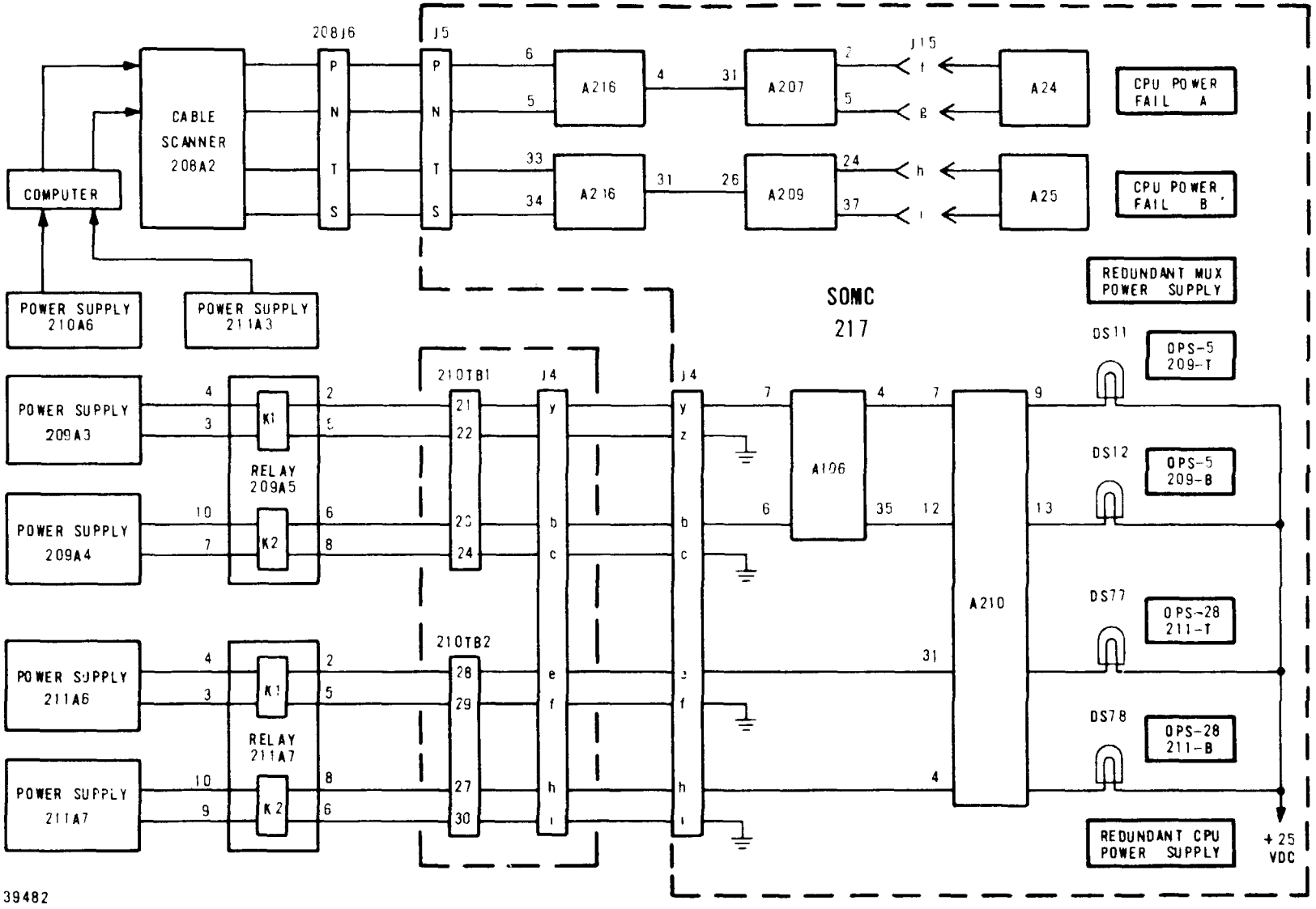

Figure 7-19. Diagram, Redundant Computer Power Supply Alarms (V7)(V8)

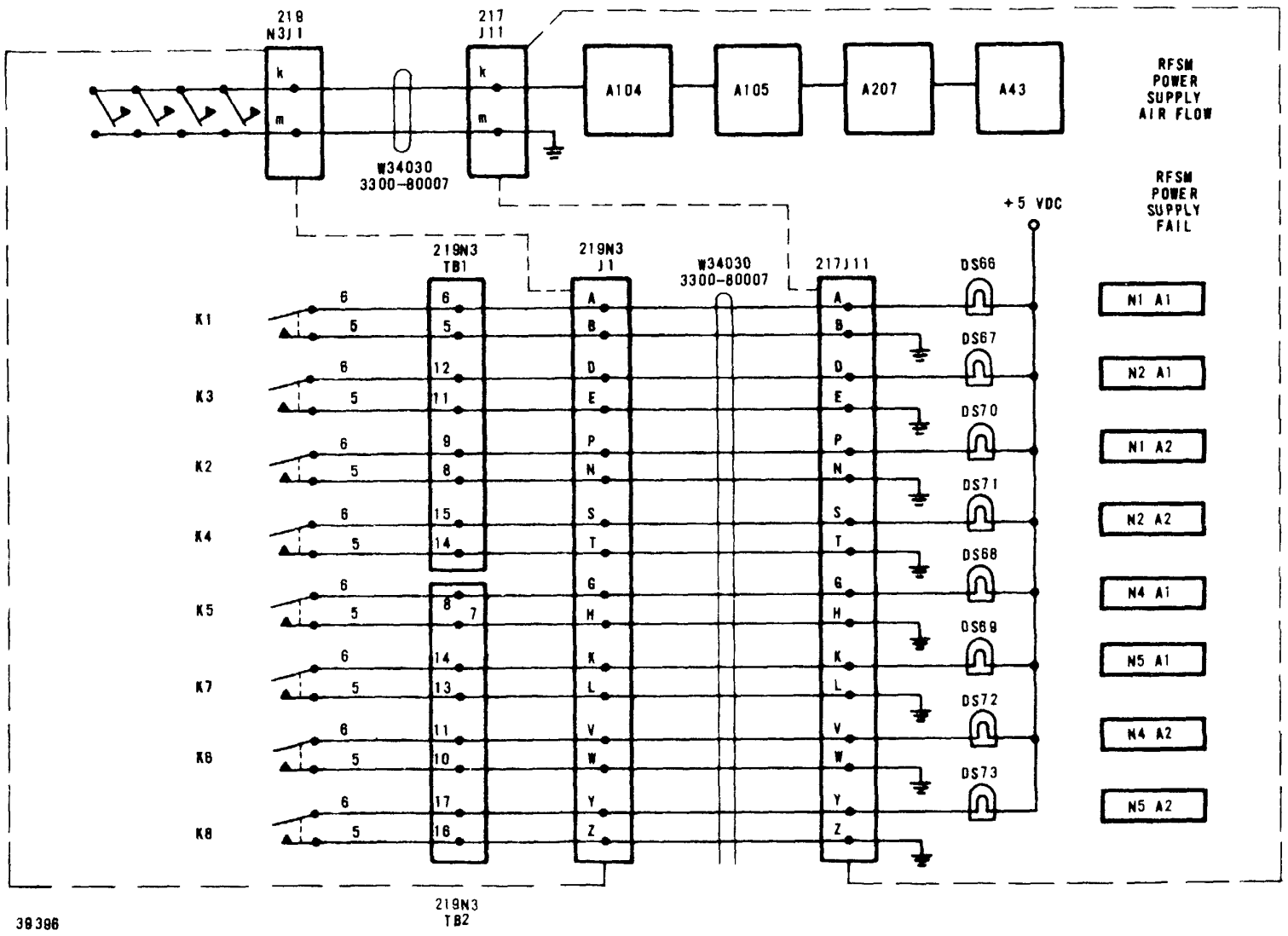

Figure 7-20. Diagram, Rfsm Power Supply Airflow and Failure Alarms (V7)

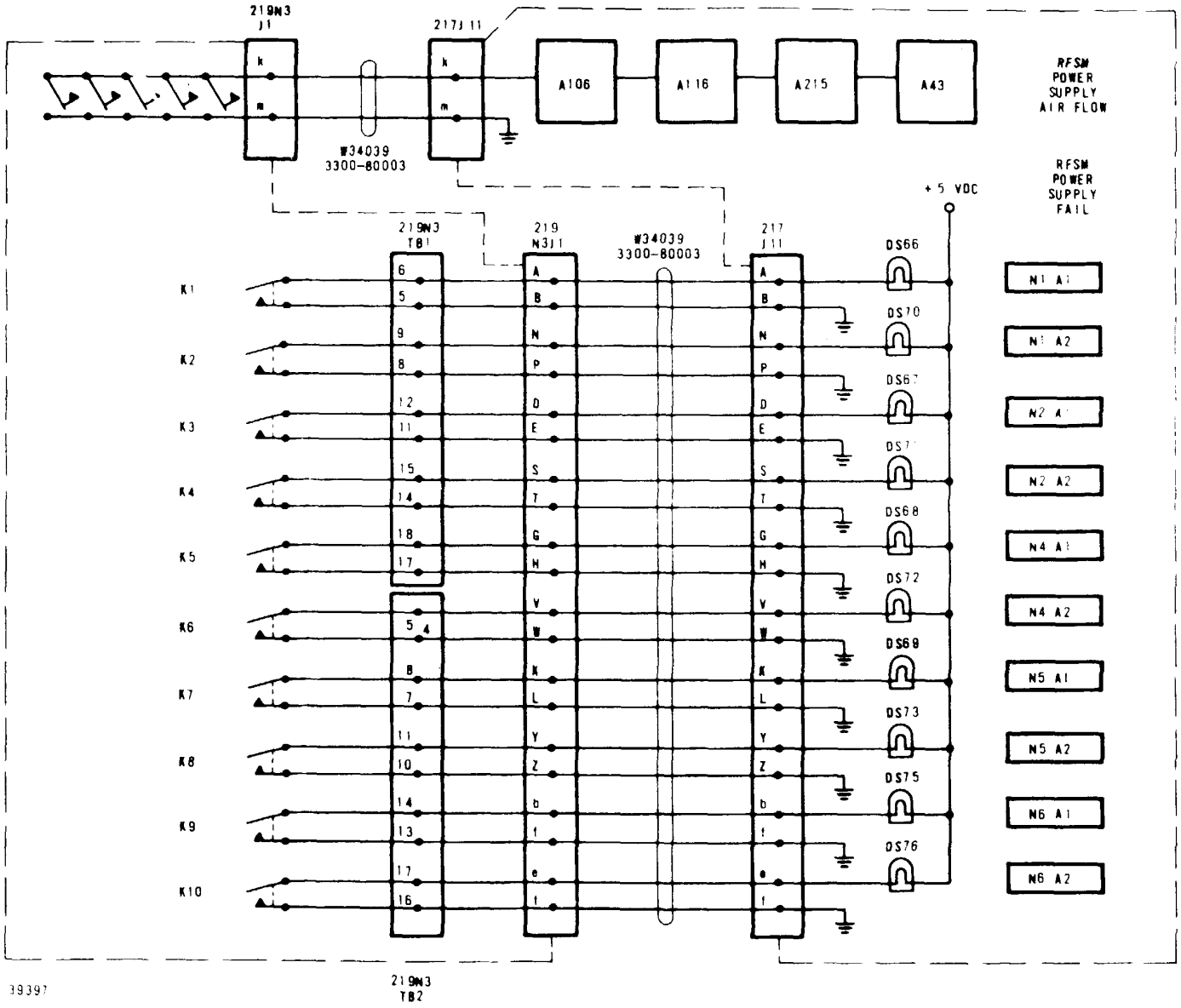

Figure 7-21. Diagram, Rfsm Power Supply Airflow and Failure Alarms (V8)

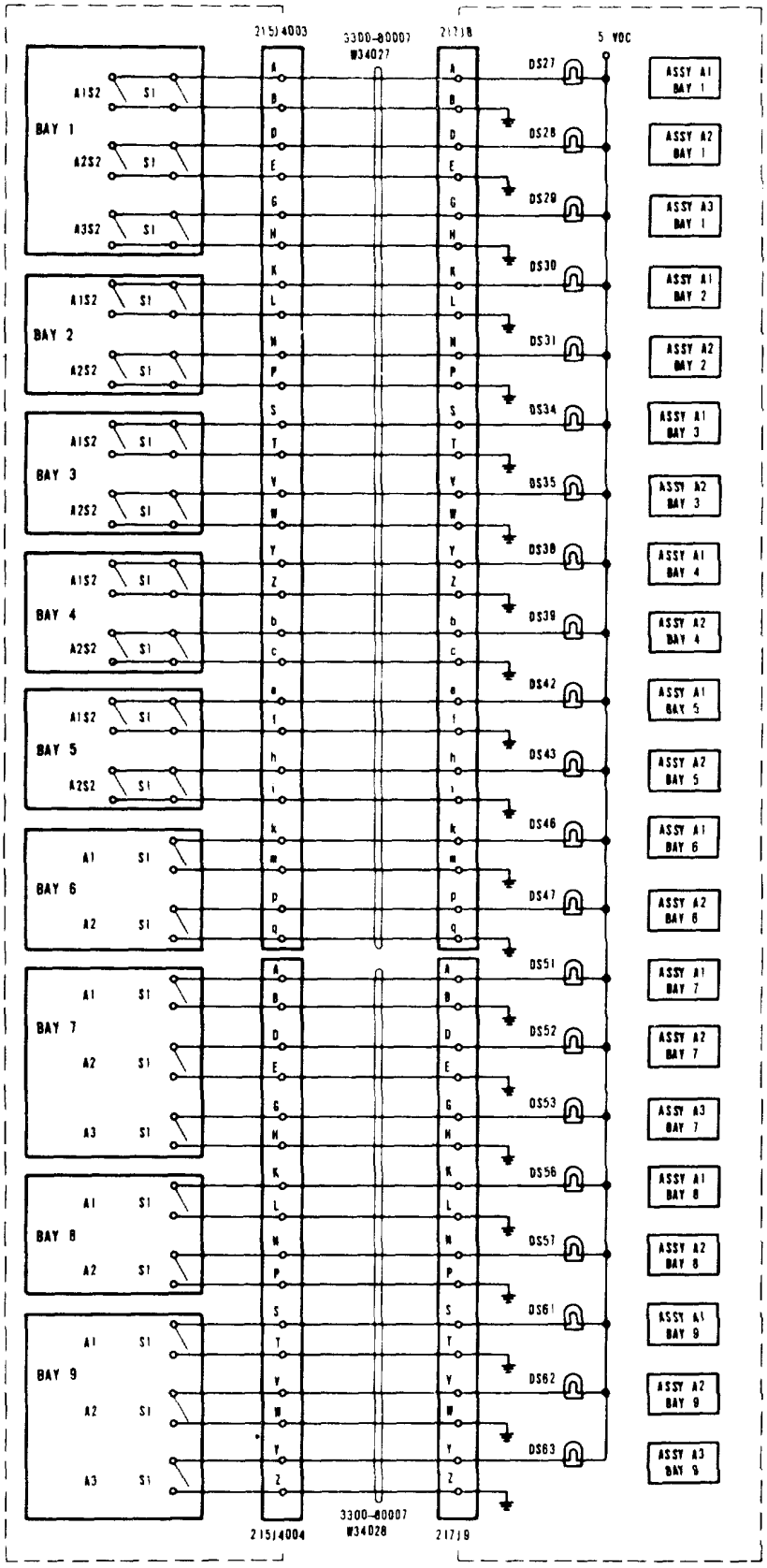

Figure 7-22. Diagram, Rfsm temperature Alarms (V7)

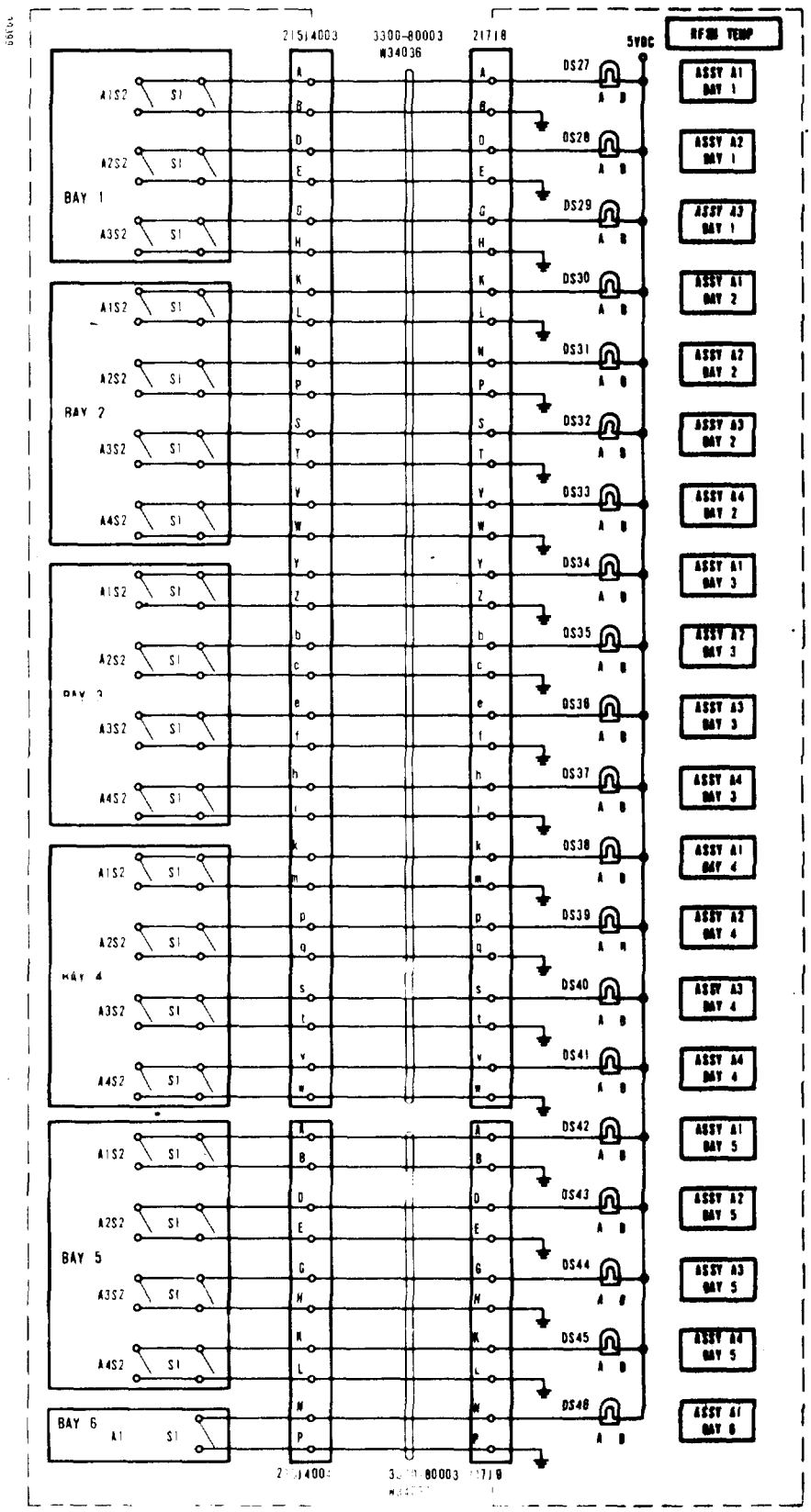

Figure 7-23. Diagram, Rfsm temperature Alarms (V8)
(Sheet 1 of 2)

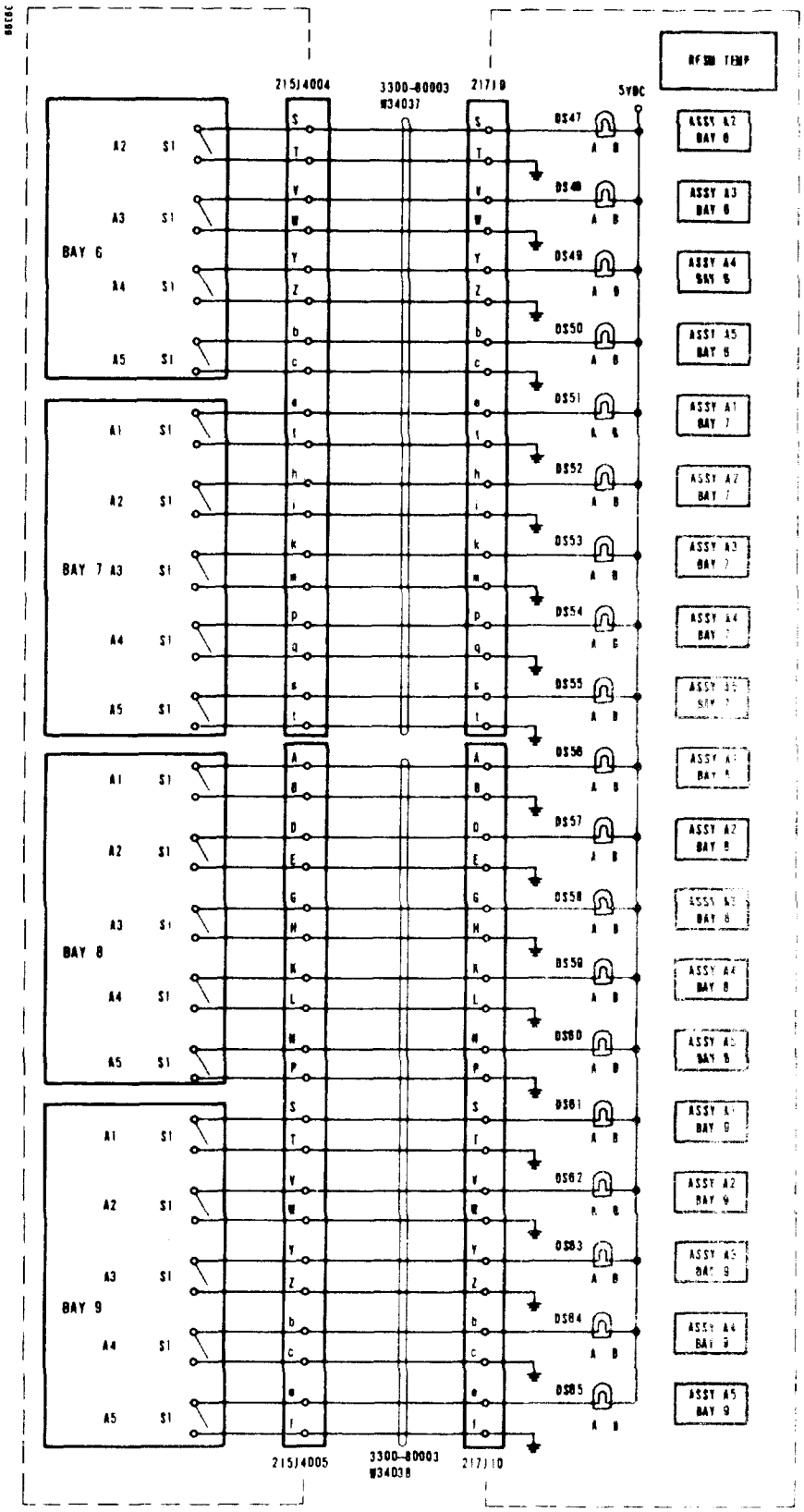

Figure 7-23. Diagram, Rfsm temperature Alarms (V8)
(Sheet 2 of 2)

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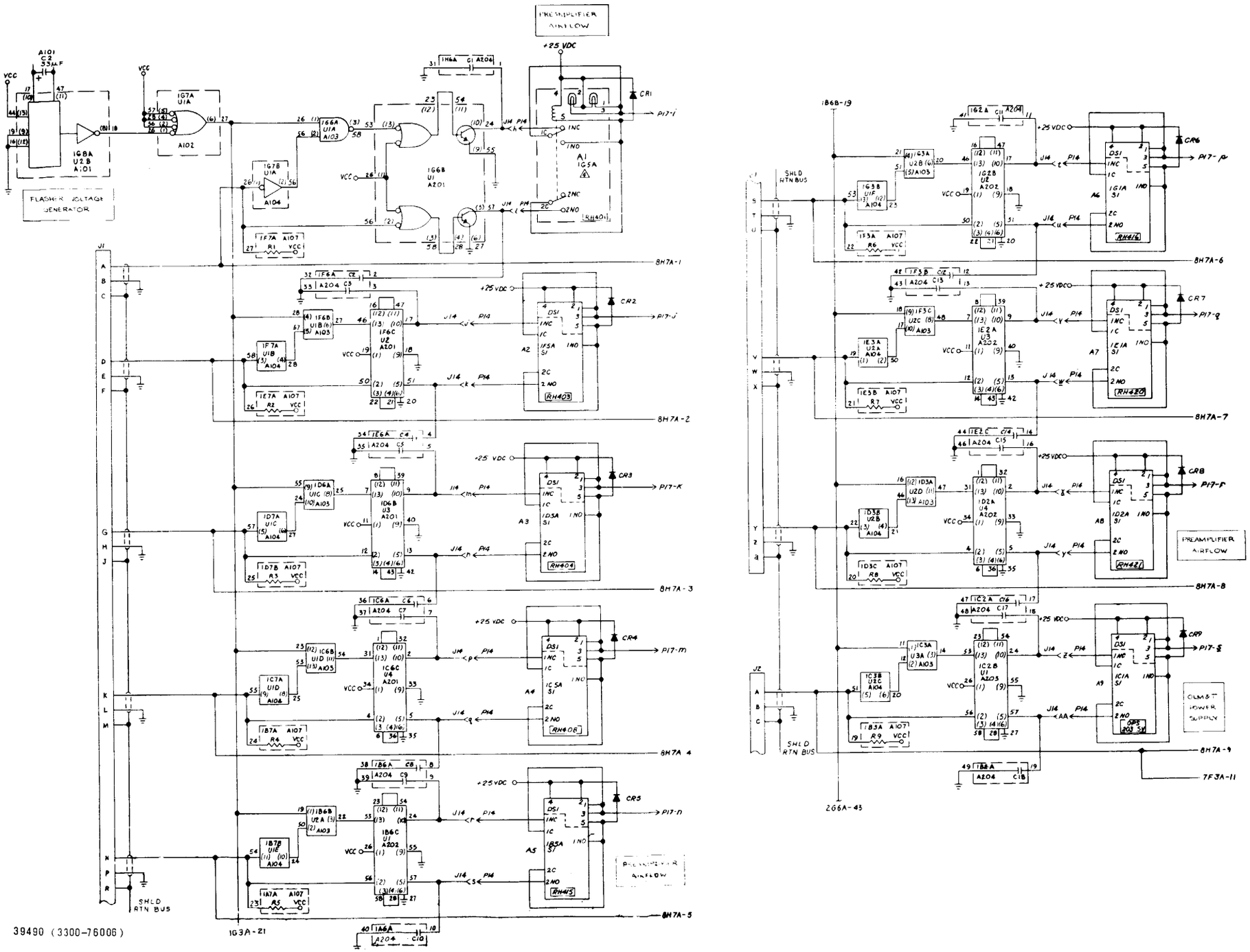

Figure 7-24. Logic Diagram, Somc Controller (V7) (Sheet 1 of 11)

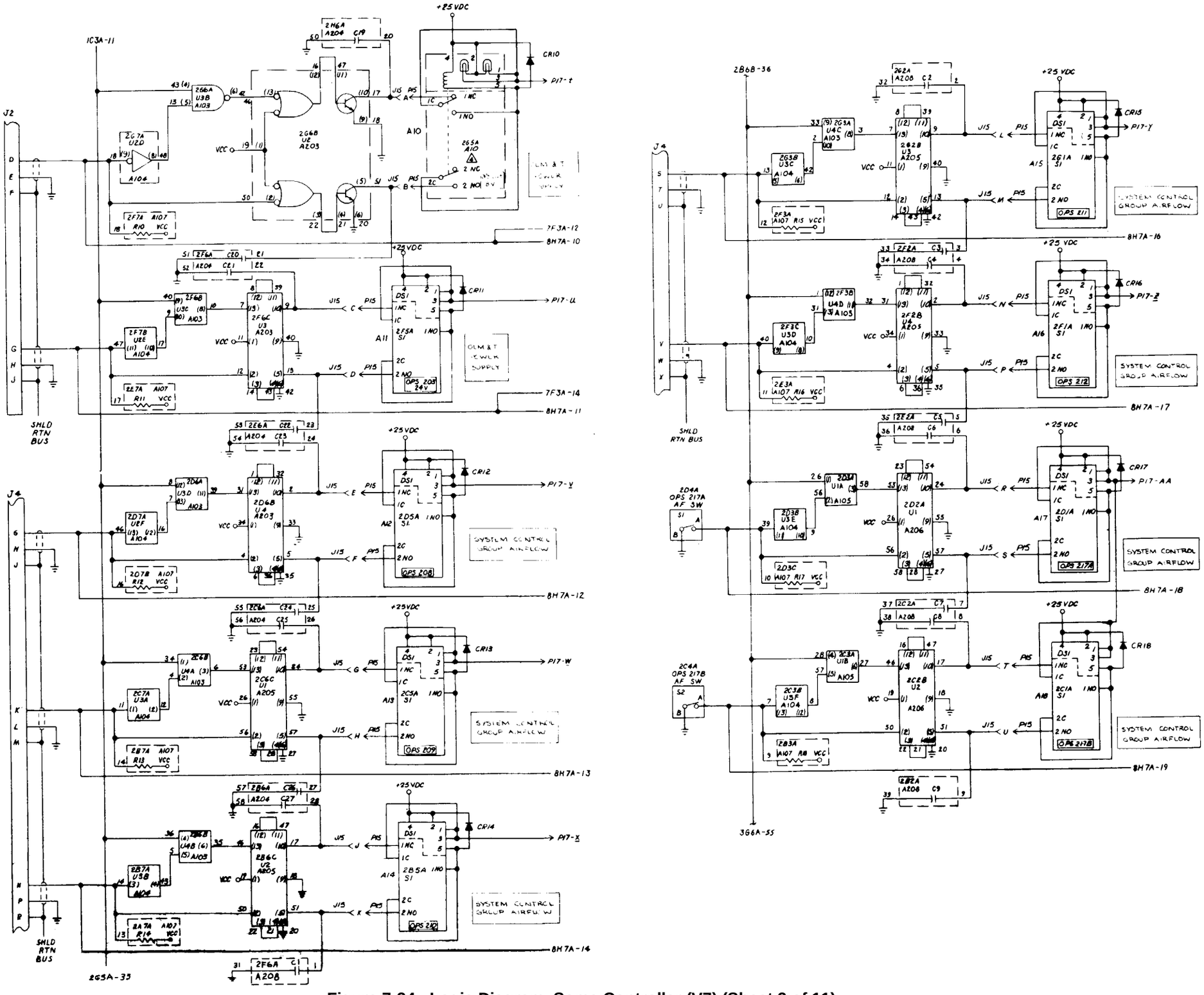

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Figure 7-24. Logic Diagram, Somc Controller (V7) (Sheet 2 of 11)

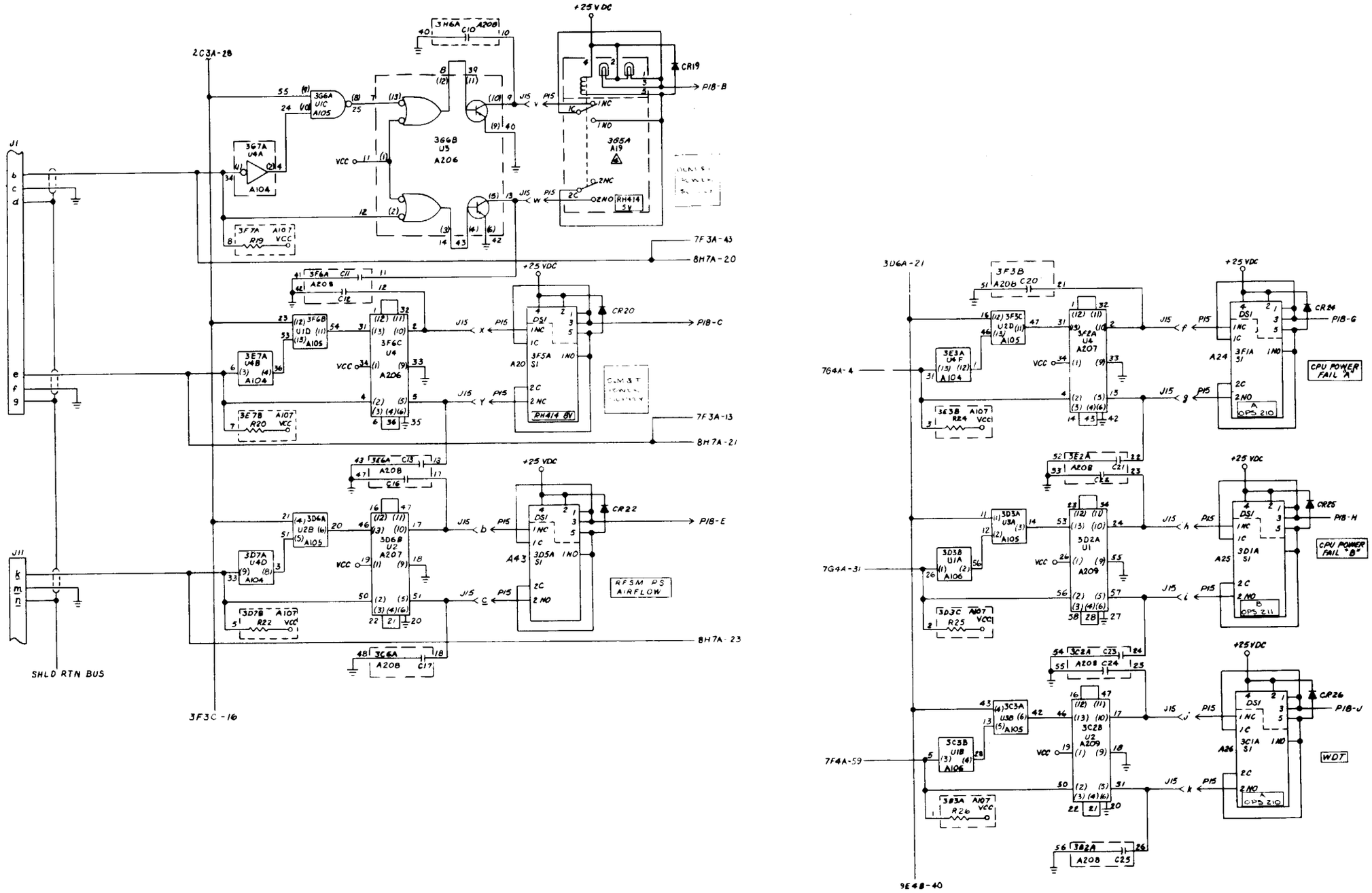

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Figure 7-24. Logic Diagram, Somc Controller (V7) (Sheet 3 of 11)

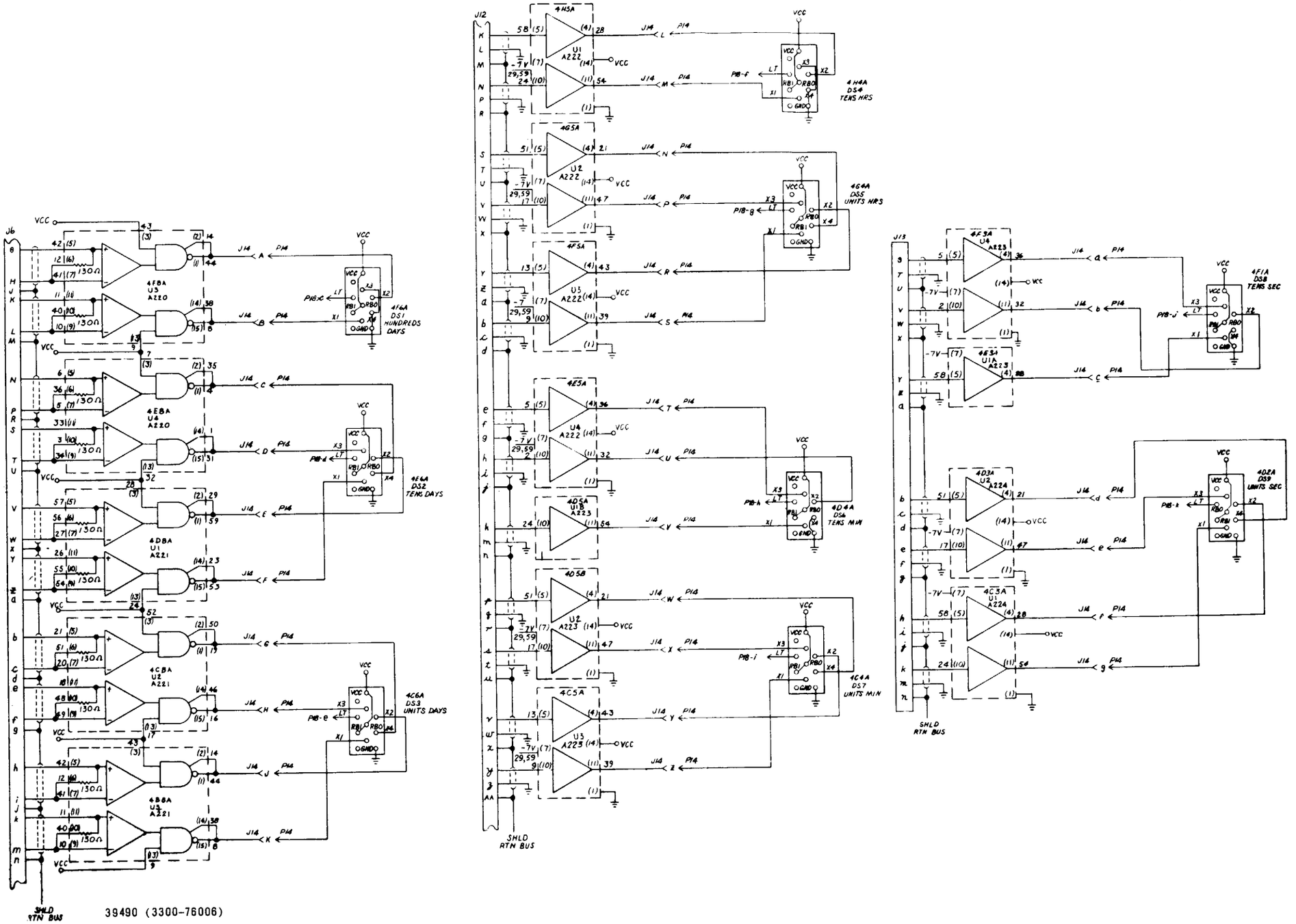

Figure 7-24. Logic Diagram, Somc Controller (V7) (Sheet 4 of 11)

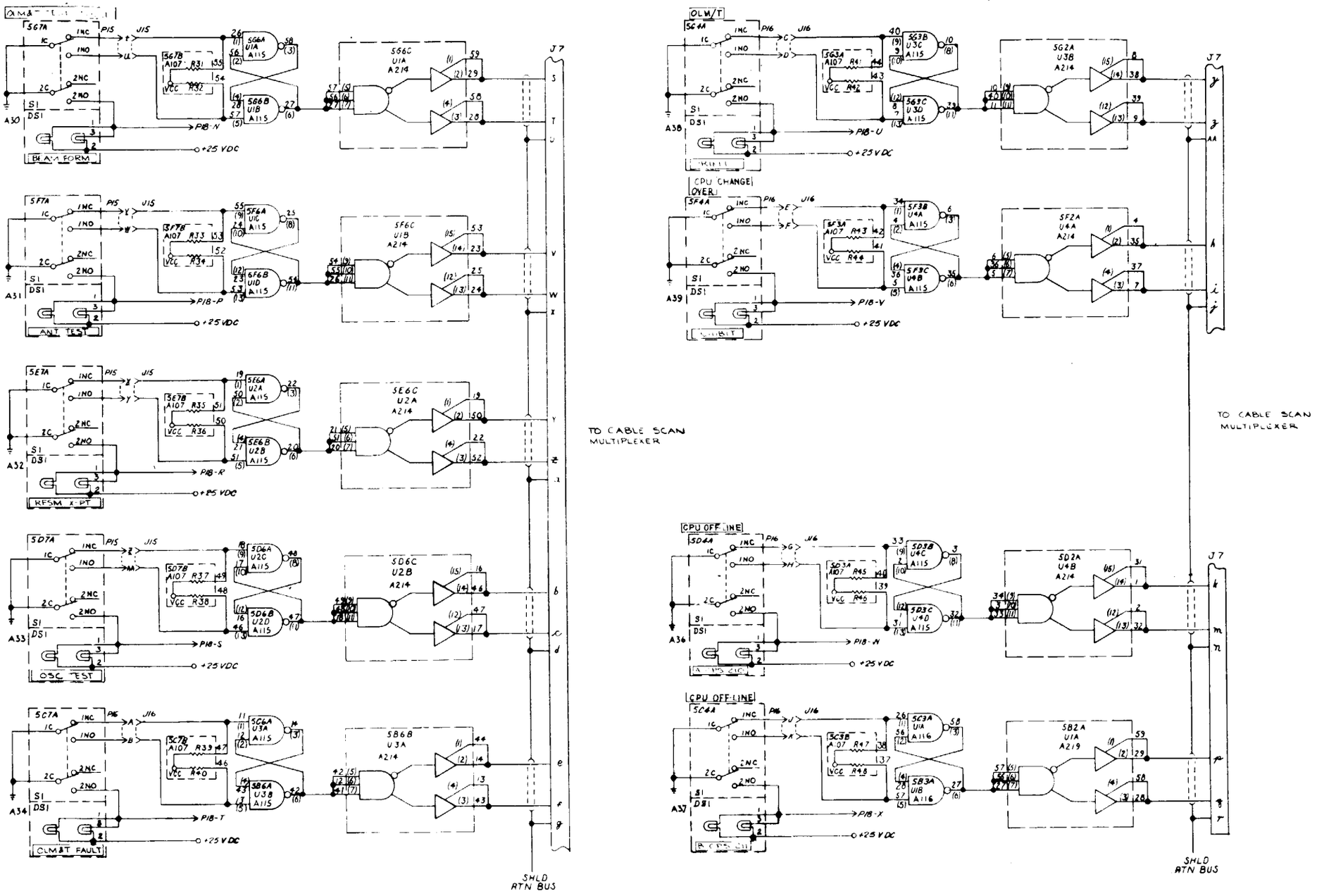

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Figure 7-24. Logic Diagram, Somc Controller (V7) (Sheet 5 of 11)

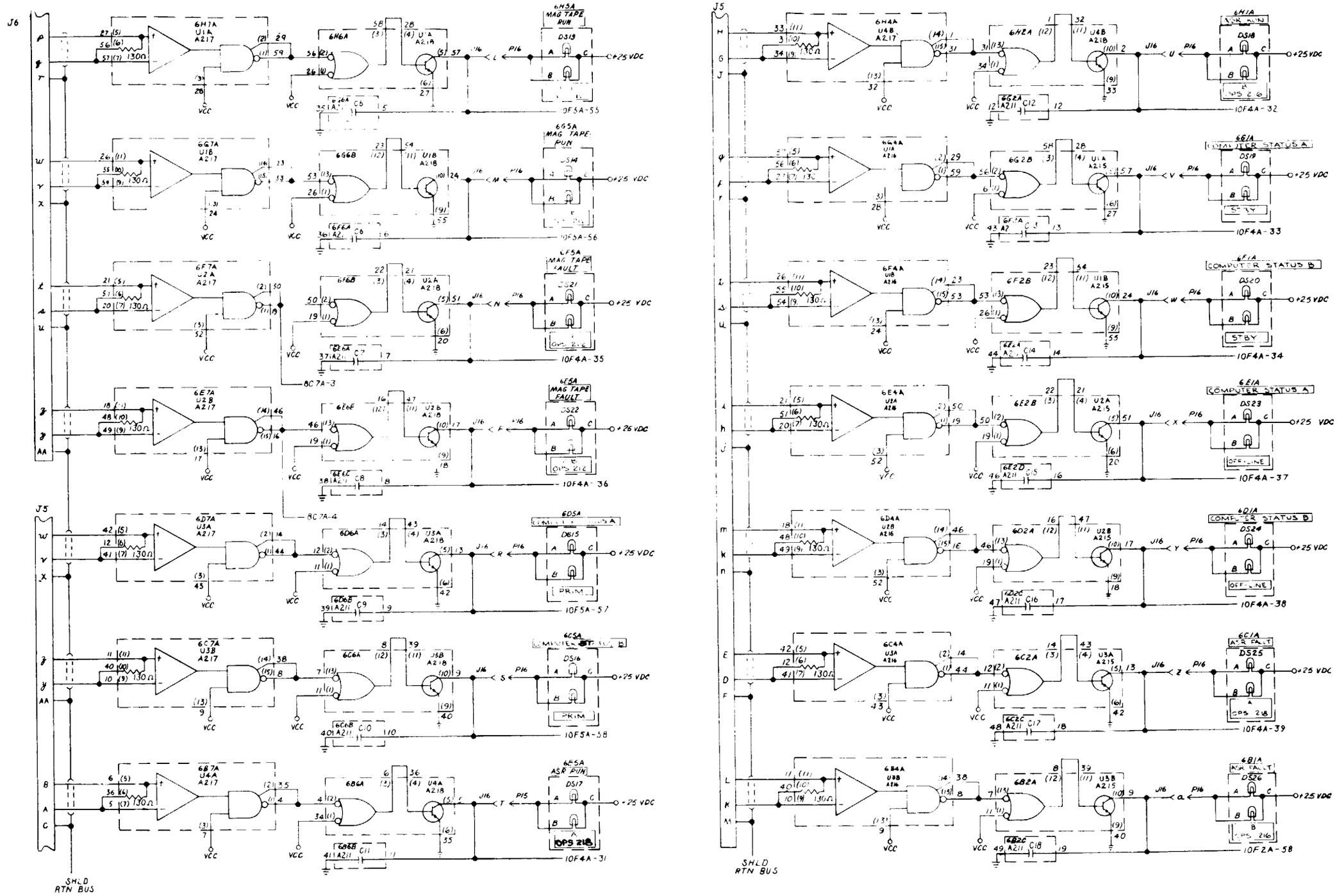

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Figure 7-24. Logic Diagram, Somc Controller (V7) (Sheet 6 of 11)

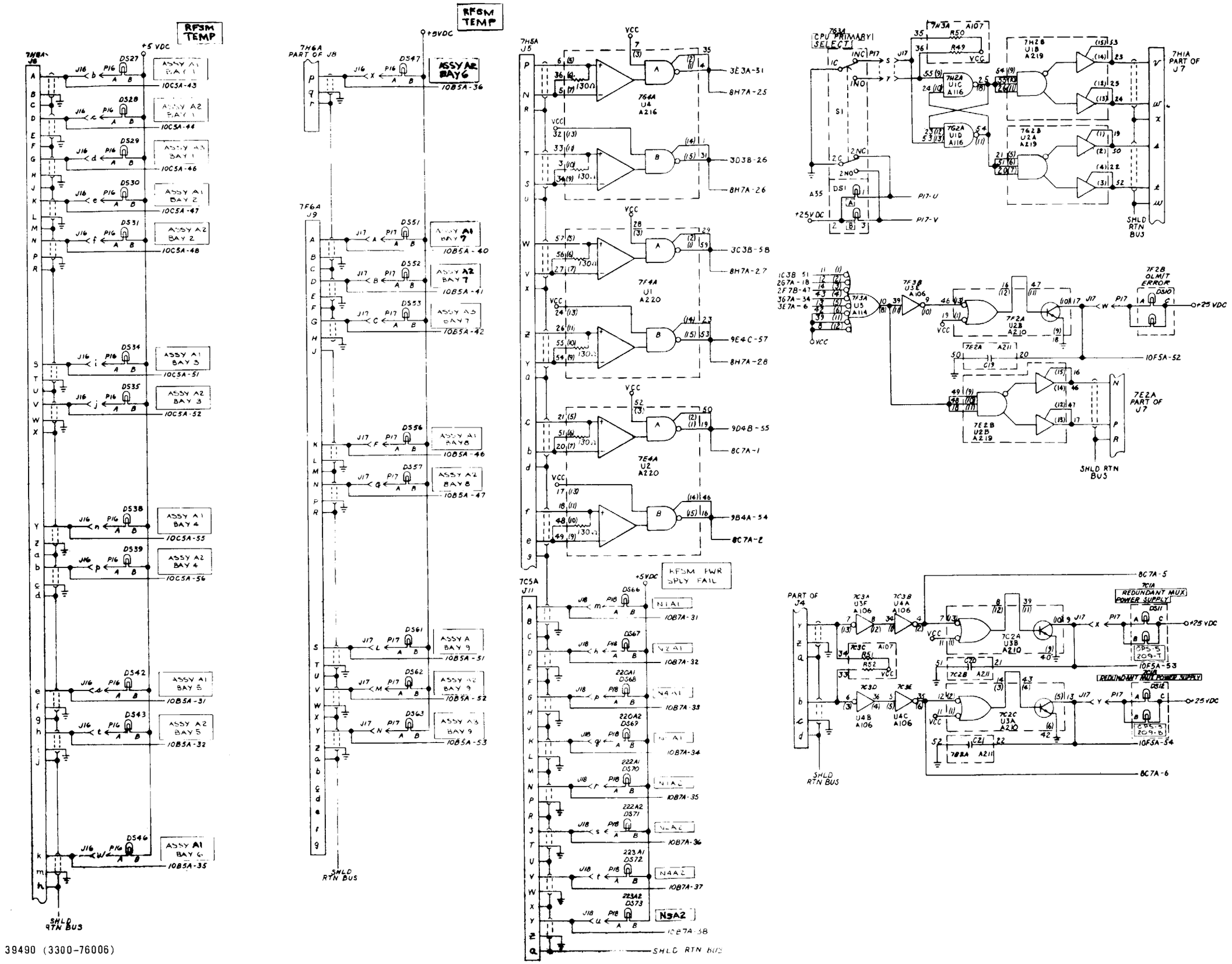

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Figure 7-24. Logic Diagram, Somc Controller (V7) (Sheet 7 of 11)

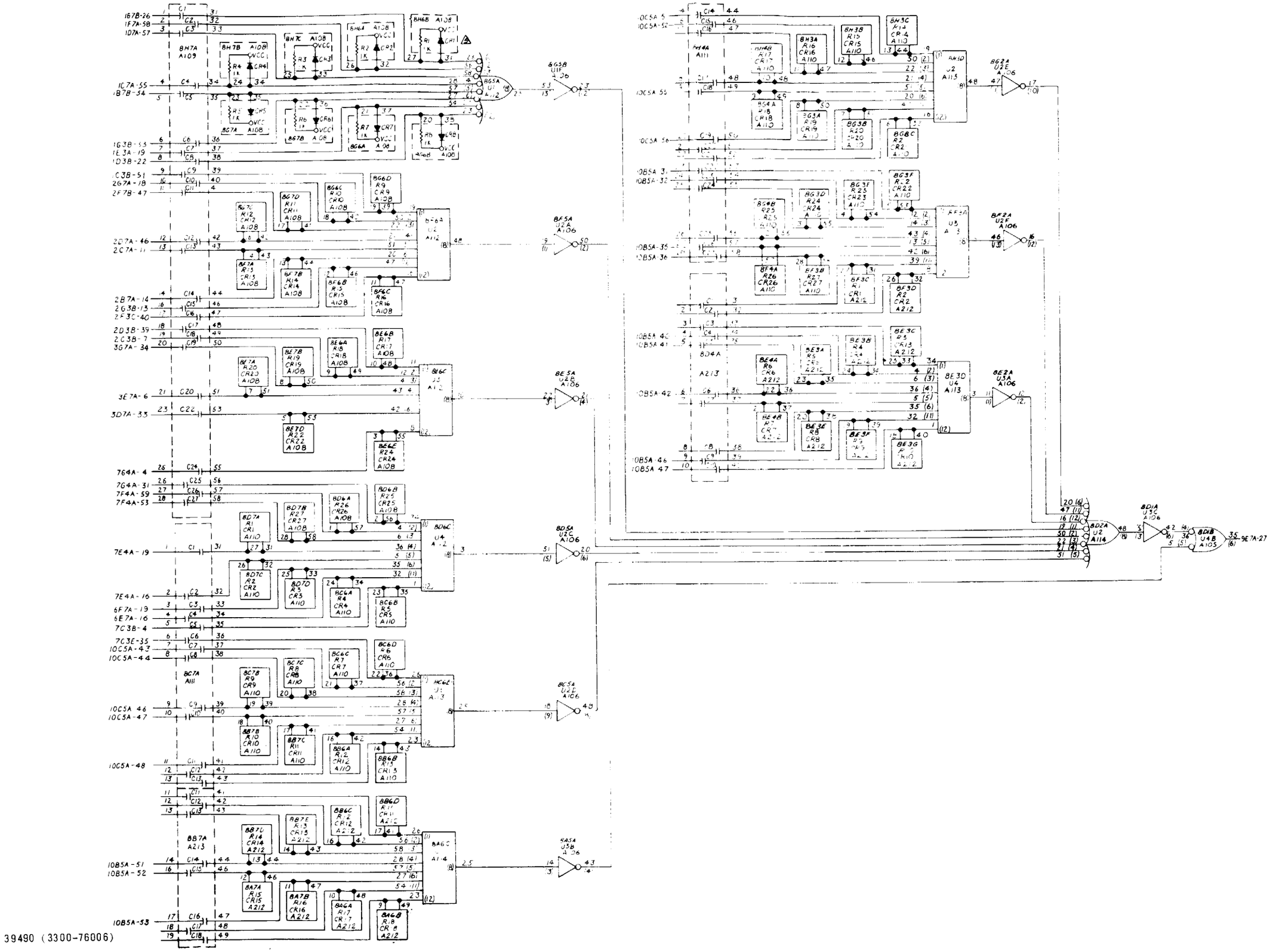

Figure 7-24. Logic Diagram, Somc Controller (V7) (Sheet 8 of 11)

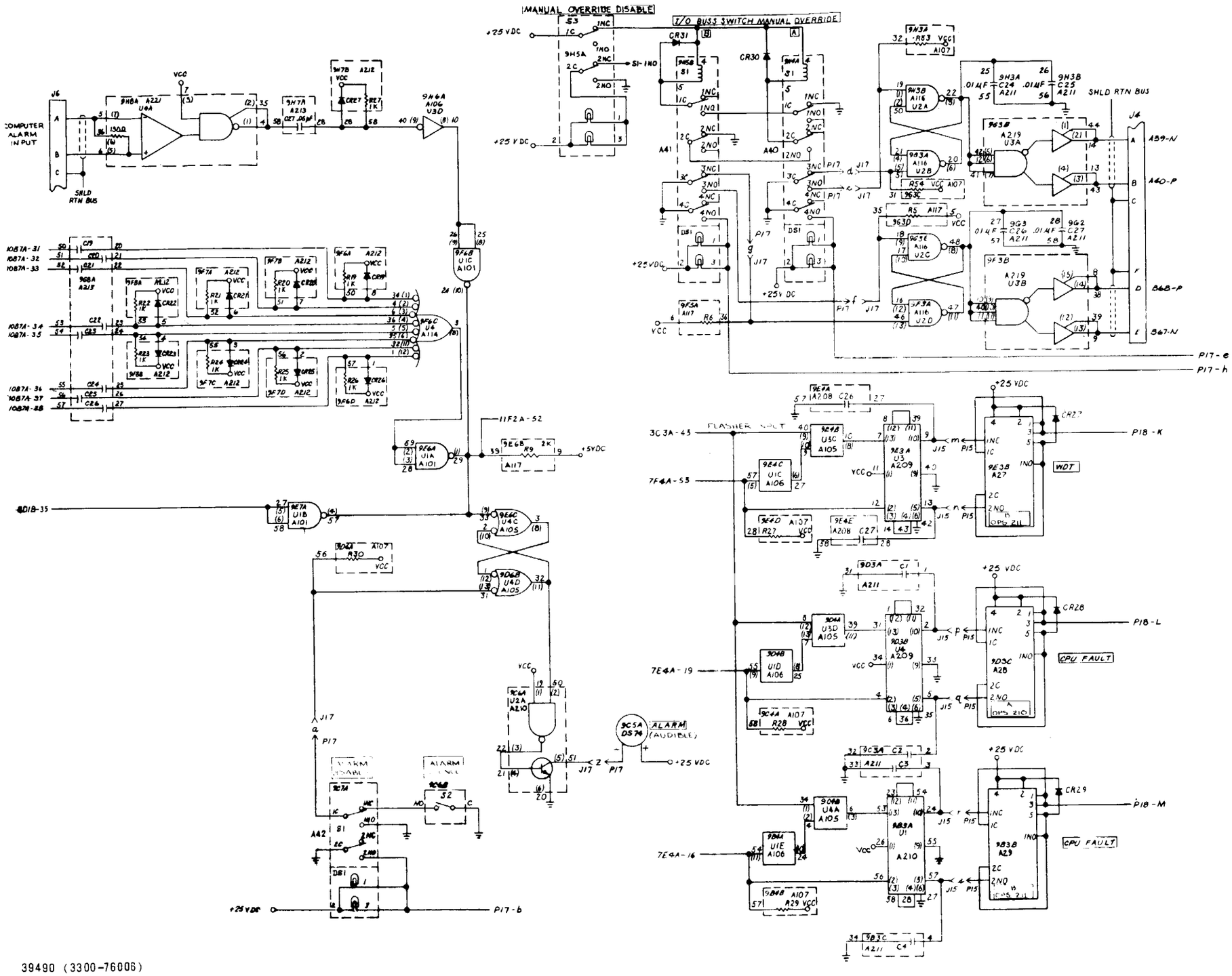

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Figure 7-24. Logic Diagram, Somc Controller (V7) (Sheet 9 of 11)

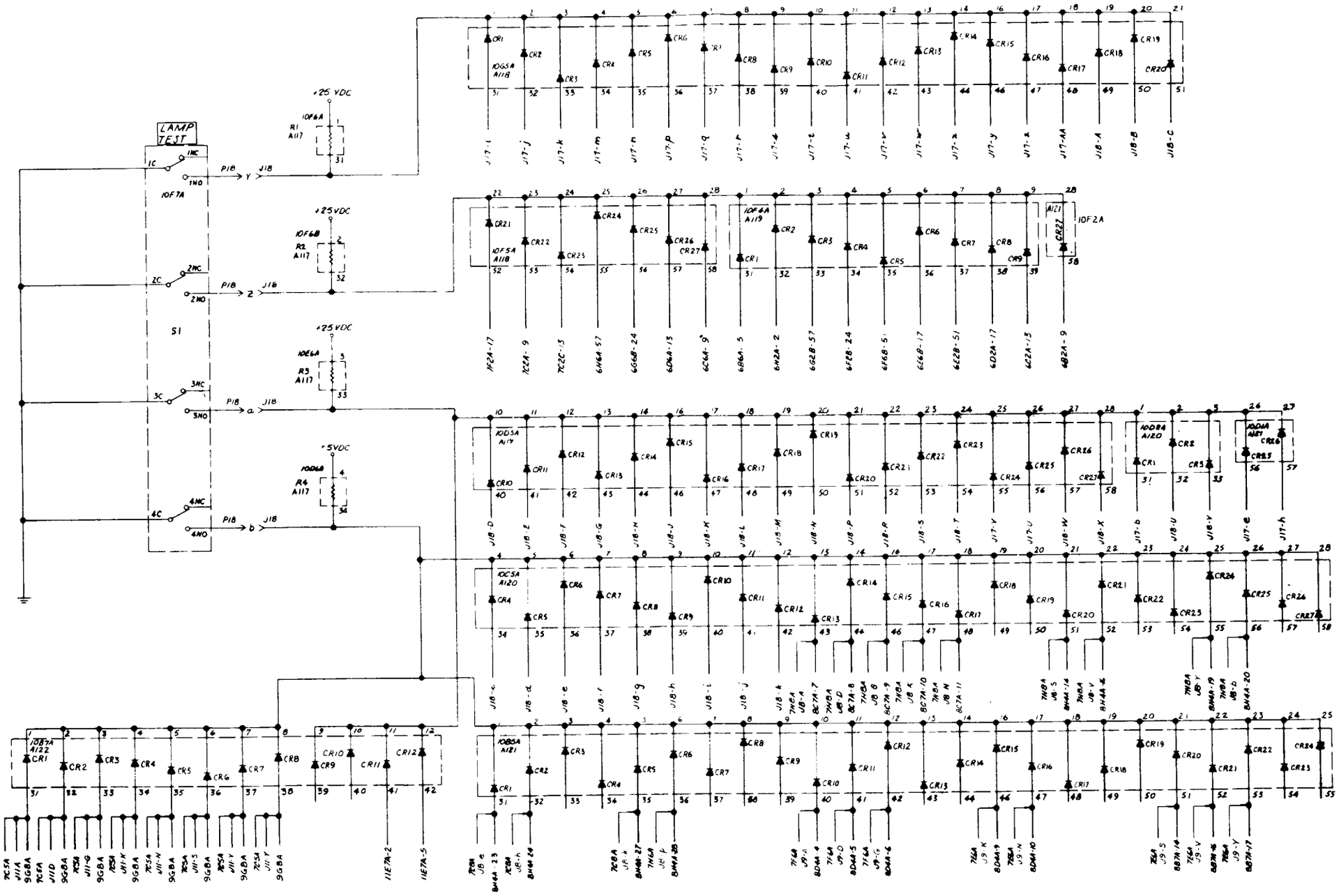

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Figure 7-24. Logic Diagram, Somc Controller (V7) (Sheet 10 of 11)

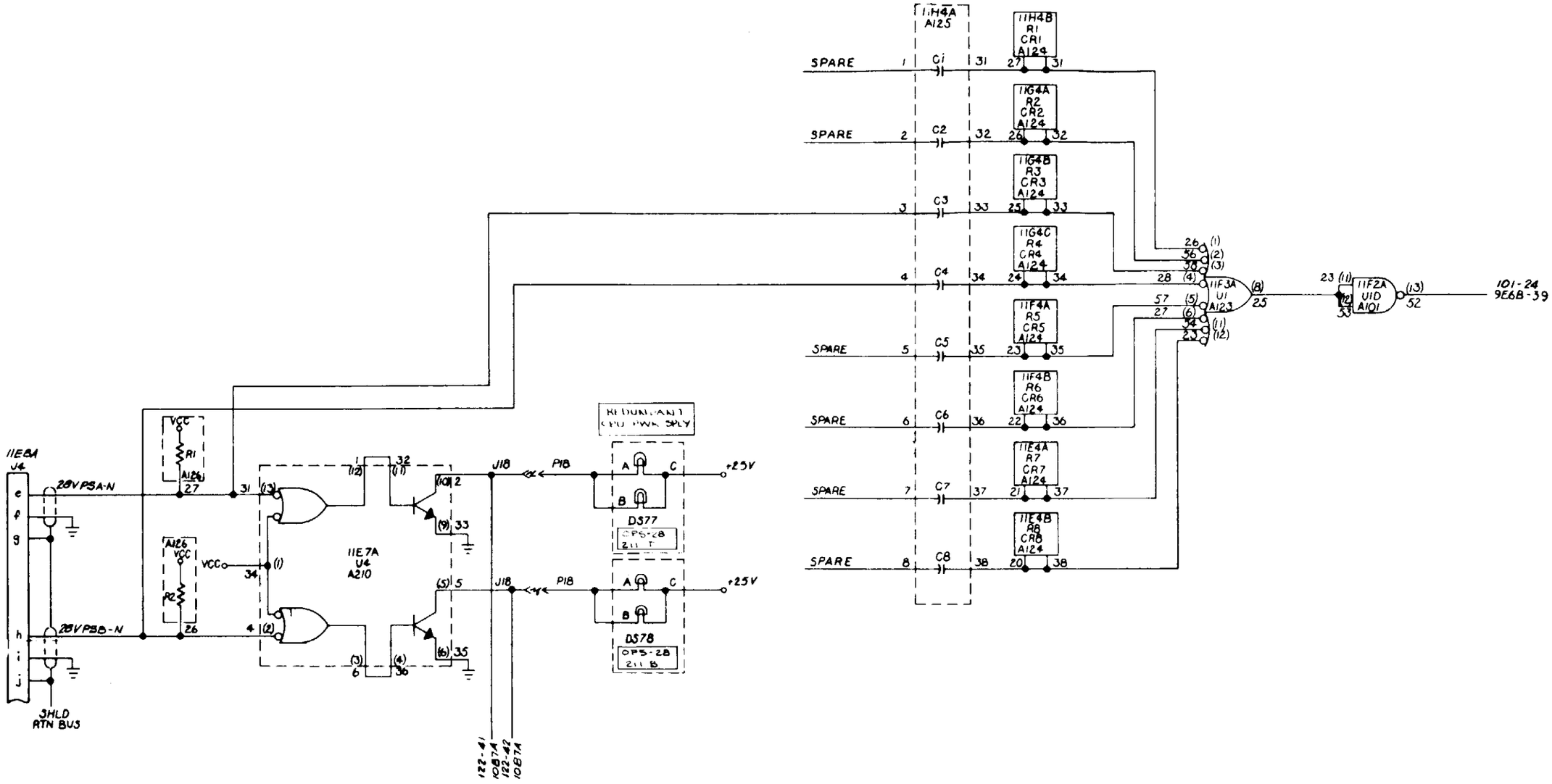

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Figure 7-24. Logic Diagram, Somc Controller (V7) (Sheet 11 of 11)

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The Metric System and Equivalents

Linear Measure

1 centimeter = 10 millimeters = .39 inch
1 decimeter = 10 centimeters = 3.94 inches
1 meter = 10 decimeters = 39.37 inches
1 dekameter = 10 meters = 32.8 feet
1 hectometer = 10 dekameters = 328.08 feet
1 kilometer = 10 hectometers = 3,280.8 feet

Weights

1 centigram = 10 milligrams = .15 grain
1 decigram = 10 centigrams = 1.54 grains
1 gram = 10 decigram = .035 ounce
1 decagram = 10 grams = .35 ounce
1 hectogram = 10 decagrams = 3.52 ounces
1 kilogram = 10 hectograms = 2.2 pounds
1 quintal = 100 kilograms = 220.46 pounds
1 metric ton = 10 quintals = 1.1 short tons

Liquid Measure

1 centiliter = 10 milliters = .34 fl. ounce
1 deciliter = 10 centiliters = 3.38 fl. ounces
1 liter = 10 deciliters = 33.81 fl. ounces
1 dekaliter = 10 liters = 2.64 gallons
1 hectoliter = 10 dekaliters = 26.42 gallons
1 kiloliter = 10 hectoliters = 264.18 gallons

Square Measure

1 sq. centimeter = 100 sq. millimeters = .155 sq. inch
1 sq. decimeter = 100 sq. centimeters = 15.5 sq. inches
1 sq. meter (centare) = 100 sq. decimeters = 10.76 sq. feet
1 sq. dekameter (are) = 100 sq. meters = 1,076.4 sq. feet
1 sq. hectometer (hectare) = 100 sq. dekameters = 2.47 acres
1 sq. kilometer = 100 sq. hectometers = .386 sq. mile

Cubic Measure

1 cu. centimeter = 1000 cu. millimeters = .06 cu. inch
1 cu. decimeter = 1000 cu. centimeters = 61.02 cu. inches
1 cu. meter = 1000 cu. decimeters = 35.31 cu. feet

Approximate Conversion Factors

To change	*To*	*Multiply by*	*To change*	*To*	*Multiply by*
inches	centimeters	2.540	ounce-inches	Newton-meters	.007062
feet	meters	.305	centimeters	inches	.394
yards	meters	.914	meters	feet	3.280
miles	kilometers	1.609	meters	yards	1.094
square inches	square centimeters	6.451	kilometers	miles	.621
square feet	square meters	.093	square centimeters	square inches	.155
square yards	square meters	.836	square meters	square feet	10.764
square miles	square kilometers	2.590	square meters	square yards	1.196
acres	square hectometers	.405	square kilometers	square miles	.386
cubic feet	cubic meters	.028	square hectometers	acres	2.471
cubic yards	cubic meters	.765	cubic meters	cubic feet	35.315
fluid ounces	milliliters	29,573	cubic meters	cubic yards	1.308
pints	liters	.473	milliliters	fluid ounces	.034
quarts	liters	.946	liters	pints	2.113
gallons	liters	3.785	liters	quarts	1.057
ounces	grams	28.349	liters	gallons	.264
pounds	kilograms	.454	grams	ounces	.035
short tons	metric tons	.907	kilograms	pounds	2.205
pound-feet	Newton-meters	1.356	metric tons	short tons	1.102
pound-inches	Newton-meters	.11296			

Temperature (Exact)

°F	Fahrenheit temperature	5/9 (after subtracting 32)	Celsius temperature	°C

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